400G QSFP-DD to 4 x 100G QSFP28 Active Optical Breakout Cable

Features

- Eight-channel full-duplex active optical cable from QSFP-DD to four QSFP28
- Supports 53.125Gb/s per channel for QSFP- DD (PAM4) and 25.78128Gb/s per channel for QSFP28 with FEC support
- Low Power Dissipation, Max 12W on QSFP- DD end, Max. 3.5W on QSFP28 end
- 8x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0℃~70
- Compliant to QSFP-DD Rev 4.0
- Compliant to Class 1M Laser Safety
- QSFP-DD form factor compliance to:

SFF-8679 electrical interface

SFF-8661 Pluggable Module

CMIS Rev. 4.0 Management Interface

IEEE 802.3cd: Physical Layer Specifications and Management Parameters

Application

- Ethernet for 4x100G
- Data Center Interconnect

Description

The QSFP-DD to 4×QSFP28 breakout AOC is an 8-channel, Pluggable, Parallel, Fiber-Optic transceiver. It is a high-performance module for short-range multi-lane data communication and interconnect applications, offering a low-cost, high-density solution for system providers and customers . This breakout cable is compliant with IEEE 802.3cd, SFF-8679, and SFF-8661 standards.

Product Specifications

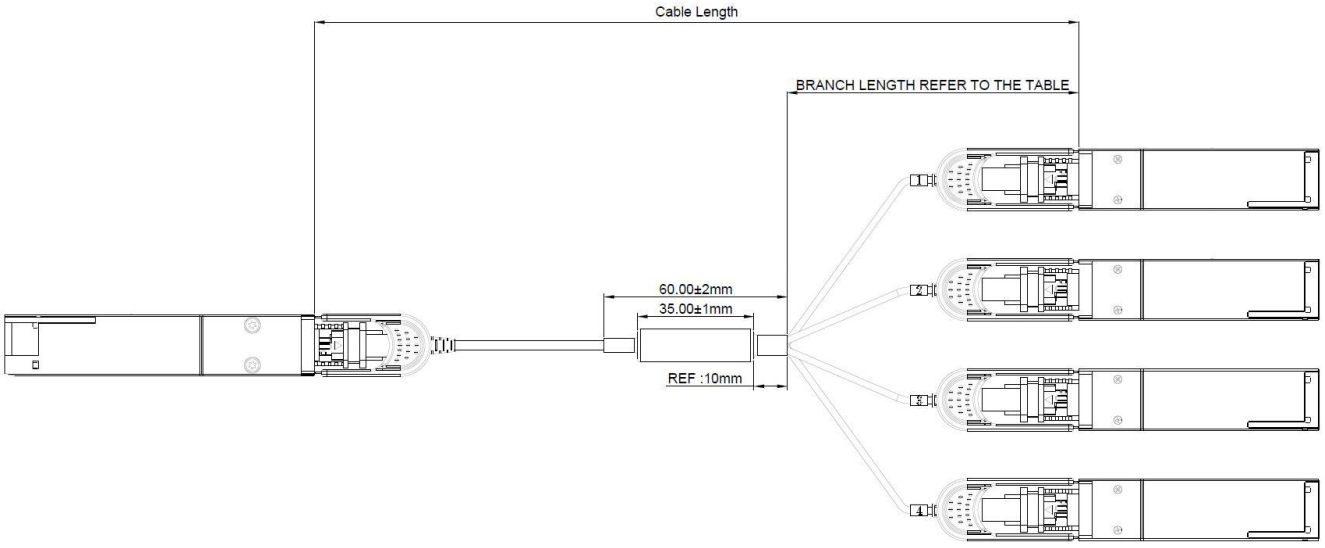
I. General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	QSFP-DD and QSFP		Module Form Factor
Number of Lanes	8TXand8RX		
Maximum Aggregate Data Rate	425(QSFP-DD) 103.1(QSFP)	Gb/s	
Maximum Data Rate per Lane	53.125	Gb/s	
Standard Cable Lengths	3, 5, 7, 10, 15, 20	meters	Other lengths maybe available upon request
Electrical Interface and Pin- out	76-pin edge connector (QSFP-DD) 38-pin edge connector(QSFP28)		Pin-out as defined byQSFP-DD Rev 4.0 & QSFPSFF8679
Maximum Power Consumption per End	12(QSFP-DD)and 3.5(QSFP28)	Watts	Varies with output voltageswing and pre-emphasis settings

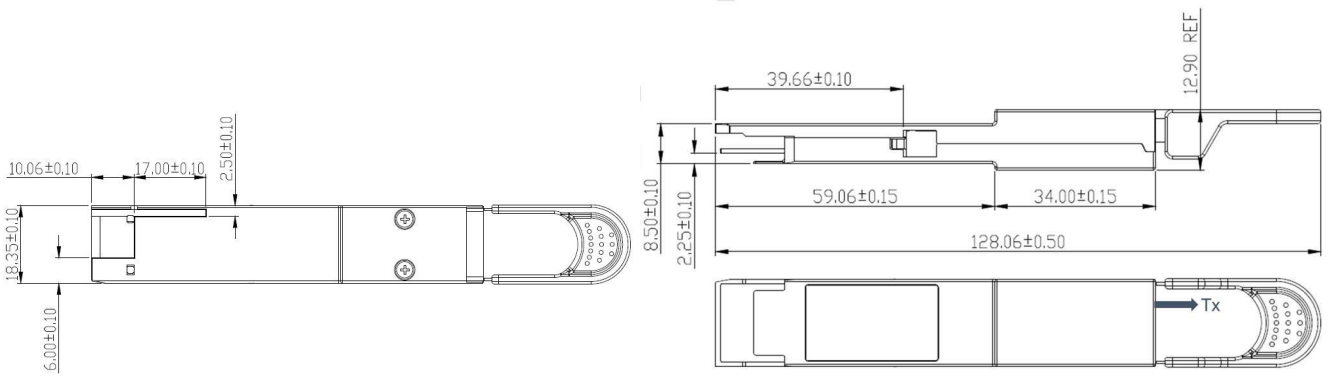
II. Force Specification

Parameter	Min.	Max.	Unit.	Comments.
Module Insertion		90(QSFP-DD) 40(QSFP28)	Newton	
ModuleExtraction		50(QSFP-DD) 30(QSFP28)	Newton	
Module Retention	90(QSFP-DD) 90(QSFP28)		Newton	
Insertion and removalcycles	50		Cycle	

III. Mechanical Specification



QSFPDD



QSFP

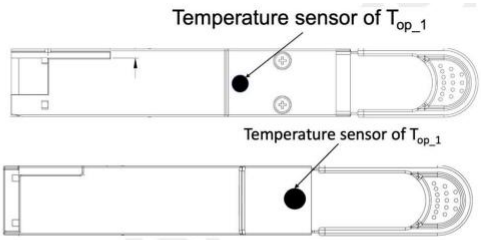
IV. Maximum Pramters

Exceeding the limits below may damage the active optical cable permanently

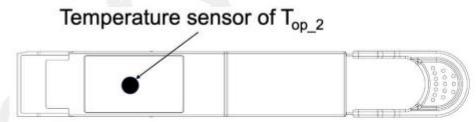
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Tsto	-40		85	℃	
Case Operating Temperature	Top_1	0		60	℃	①、②
	Top_2	0		70	℃	②
Relative Humidity	RH	5		85	%	

1. DDMI temperature reading is measured by the position of Top_1
2. Case operating temperature definition:

Top view of module:



Bottom view of module:



V. Recommended Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Supply Voltage	Vcc	3.14		3.46	V	
Power Consumption	PCon			12(QSFP-DD) 3.5(QSFP28)	W	
Optical Data Rate (PAM4)	BR		26.5625		GBd	①
Electrical Data Rate for QSFP28 (NRZ)	BR		25.78125		Gb/s	
Center wavelength	λc	840		860	nm	②
Pre-FEC Bit Error Rate (PAM4)				2.4x10-4		③
Pre-FEC Bit Error Rate (NRZ)				5x10-5		

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Post-FEC Bit Error Rate				1x10-12		
Beam divergence angle			23		°	
Number of Lanes			8			
Management Interface		Serial,I2C-based,maximumfrequency 400kHz				④
Logic Input Voltage High	Vih	2		Vcc+0.3	V	
Logic Input Voltage Low	Vil	-0.3		0.8	V	

① Single lane
② PRBS31Q test pattern is used.
③ As defined by IEEE Std. 802.3bs ™/D3.5
④ As defined by SFF-8636

VI. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
TransmitteratTP1a						
AC common-mode output voltage (RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitterdisabled)				35	mV	
Differential peak-to-peak output voltage (Transmitterenabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eyeheight,differential	EH	32			mV	
Differentia loutput returnloss		SeeEq.1				
Common to differential mode conversion return loss		SeeEq. 2				
Differential termination mismatch		10			%	
Transition time (20%to80%)	Tr,Tf			10	ps	
Receiverat TP4						
Far-end Eye height,differential		30			mV	
Far-end pre-cursorISIratio		-4.5		2.5	%	
Differential output return loss		SeeEq.1				
Common to differential mode conversion return loss		SeeEq. 2				
Differential ermination mismatch		10			%	

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transitiontime(20%to80%)	Tr,Tf	10			ps	
DCcommon modevoltage		-350		2850	mV	

1. $RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases}$ (dB) (Eq.1)

where

f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

2. $RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases}$ (dB) (Eq.2)

where

f is the frequency in GHz,

RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
TransmitteratTP1a						
Differential Data Output Voltage Peak to Peak Swing	Vin,pp			900	mV	
Differential Input Return Loss	SDD22	Per OIF CEI-28G-VSR and CAUI-4 Requirements			dB	
Common Mode to Differential Conversion and Differential to Common Mode Conversion	SDD22 SCD22				dB	
Common Mode Return Loss	SCC22				dB	
Transition Time,20% to 80%	Tr,Tf	10			ps	
Common Mode Voltage	Vcm	-0.3		2.8	V	
Receiverat TP4						
Differential Data Output Voltage Peak to Peak Swing	Vopp			900	mV	
Differential Output Impedance	Zos	90	100	110	Ohms	
Common Mode Voltage	Vcm	-0.35		2.85	V	①
Differential Output Return Loss	SDD22	Per OIF CEI-28G-VSR and CAUI-4 Requirements			dB	
Common Mode to Differential Conversion and Differential to Common Mode Conversion	SDD22 SCD22					
Common Mode Return Loss	SCC22			-2	dB	②
Transition Time,20% to 80%	Tr,Tf	10			ps	
Eye Width @1E-15 Probability	EW15	0.57			UI	
Eye Height@1E-15P robability	EH15	228			mV	

① Vcm is generated by the host. Specification includes effects of ground offset voltage.
② From 250MHz to 30GHz

VII. PIN DESCRIPTIONS (compliant QSFP-DD Rev. 4.0)

PIN	Symbol	Description	Ref.
1	GND	Ground	Ⓒ
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	Ⓒ
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	Ⓒ
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRX	+3.3VPower Supply Receiver	Ⓒ
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	Ⓒ
14	RX3p	ReceiverNon-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	Ⓒ
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	Ⓒ
20	GND	Ground	Ⓒ
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	Ⓒ
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	Ⓒ
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTX	+3.3V Power supply transmitter	Ⓒ

PIN	Symbol	Description	Ref.
30	Vcc1	+3.3V Powersupply	Ⓒ
31	LPMode	Initializationmode;Inlegacy QSFP applications, the InitMode pad is called LPMODE	
32	GND	Ground	Ⓒ
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	Ⓒ
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	Ⓒ
39	GND	Ground	Ⓒ
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	Ⓒ
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted DataInput	
45	GND	Ground	Ⓒ
46	Reserved	Forfutureuse	③
47	VS1	Module Vendor Specific1	③
48	3.3VPowerSupply	2A	②
49	VS2	Module Vendor Specific2	③
50	VS3	Module Vendor Specific3	③
51	GND	Ground	Ⓒ
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	Ⓒ
55	Rx5p	Receiver Non-Inverted DataOutput	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	Ⓒ
58	GND	Ground	Ⓒ
59	Rx6n	Receiver InvertedData Output	
60	Rx6p	Receiver Non-Inverted DataOutput	
61	GND	Ground	Ⓒ
62	Rx8n	Receiver Inverted Data Output	

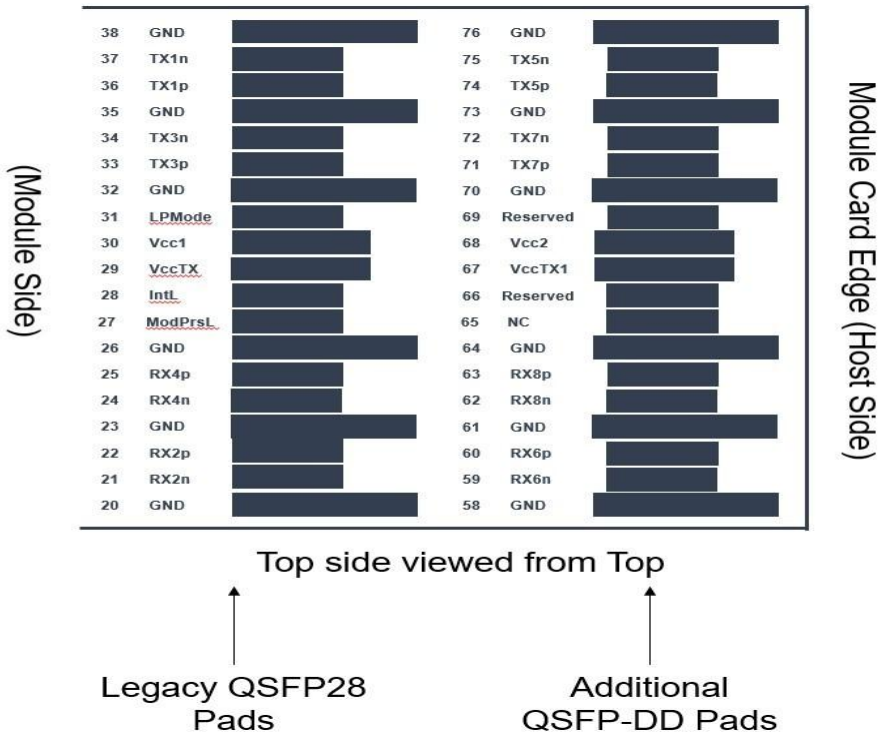
PIN	Symbol	Description	Ref.
63	Rx8p	Receiver Non-Inverted DataOutput	
64	GND	Ground	ⓒ
65	NC	No Connect	③
66	Reserved	For future use	③
67	VccTx1	3.3V Power Supply	②
68	Vcc2	3.3V Power Supply	ⓒ
69	Reserved	For Future Use	③
70	GND	Ground	ⓒ
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	ⓒ
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	ⓒ

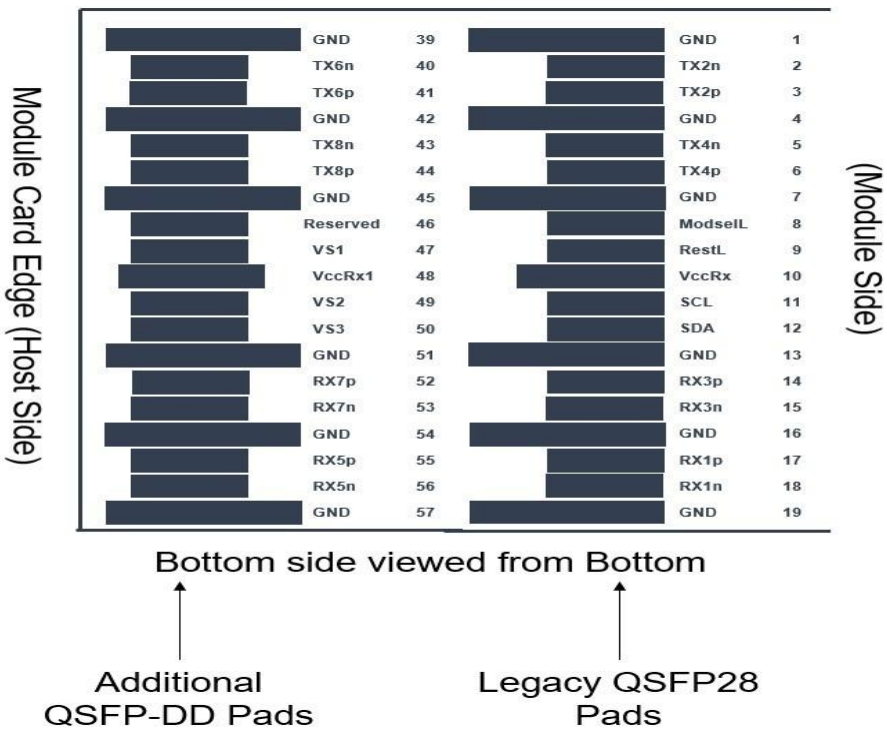
① QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

② VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc ping are each rated for a maximum current of 1000 mA.

③ All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to grounds on the host. Pad 65 (No connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.

④ Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, the break contact with additional QSFP- DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.


(Module Side)
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 LPMode
30 Vcc1
29 VccTX
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 Reserved
68 Vcc2
67 VccTX1
66 Reserved
65 NC
64 GND
63 RX8p
62 RX8n
61 GND
60 RX6p
59 RX6n
58 GND
Module Card Edge (Host Side)
Top side viewed from Top
Legacy QSFP28 Pads
Additional QSFP-DD Pads


Module Card Edge (Host Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModselL 8
RestL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19
(Module Side)
Bottom side viewed from Bottom
Additional QSFP-DD Pads
Legacy QSFP28 Pads

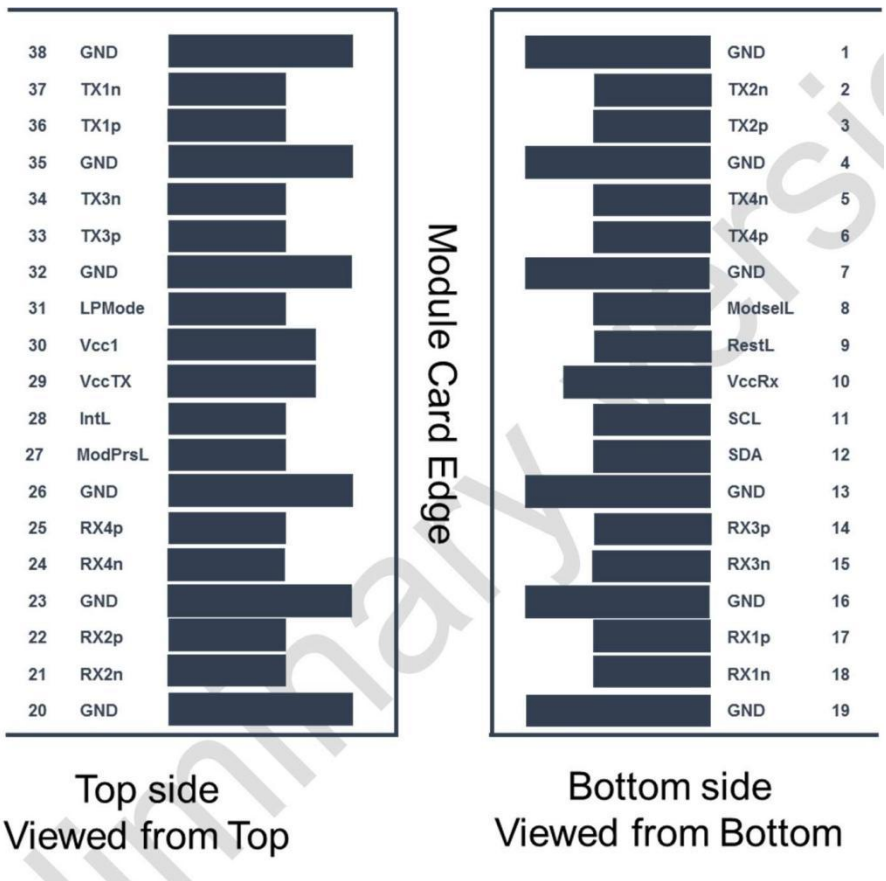
VII. PIN DESCRIPTIONS (compliant SFF-8679)

PIN	Symbol	Description	Ref.
1	GND	Ground	
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	TransmitterNon-Inverted Data Input	
4	GND	Ground	©
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted DataInput	
7	GND	Ground	©
8	ModSelL	Module Select	©
9	ResetL	Module Reset	©
10	VccRX	+3.3V Receiver Power Supply Receiver	
11	SCL	2-wire Serial Interface Clock	©
12	SDA	2-wire Serial Interface Data	©
13	GND	Ground	©
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	©
17	RX1p	Receiver Non-Inverted DataOutput	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	©
20	GND	Ground	©
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	©
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted DataOutput	
26	GND	Ground	©
27	ModPrsL	Module Present,internal pulled down to GND	
28	IntL	Interrupt output,should be pulled up on host board	
29	VccTX	+3.3VTransmitterPowerSupply	
30	Vcc1	+3.3V Power Supply	
31	LPMode	LowPowerMode	©
32	GND	Ground	

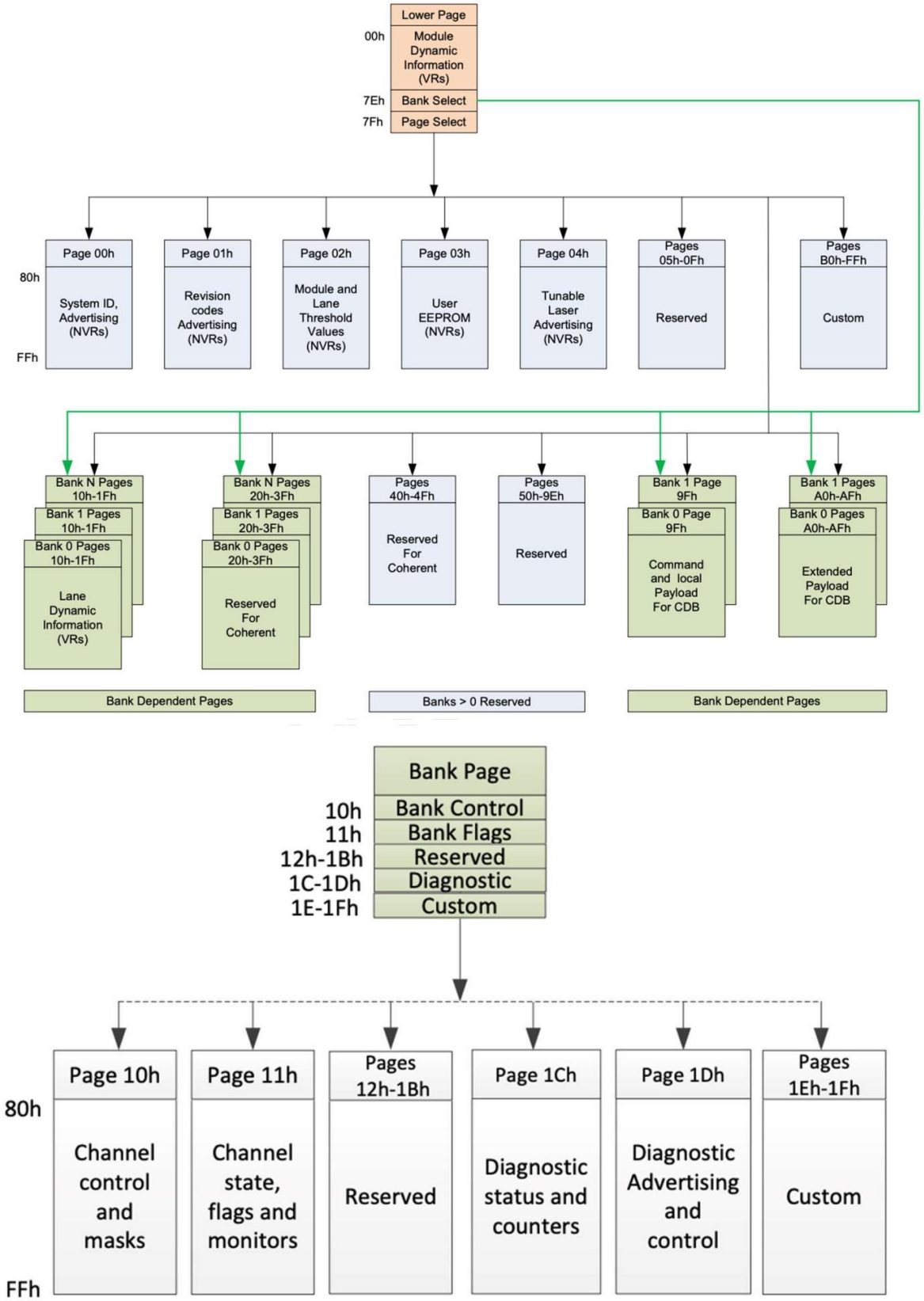
PIN	Symbol	Description	Ref.
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	©

① GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are reference to this potential unless otherwise noted. Module circuit ground is isolated from module chassis ground within the module.

② Open collector, should be pulled up with 4.7~10K ohms on the host board to a voltage between 3.15V and 3.6V.



MEMORY MAP (compliant CMIS Rev4.0)

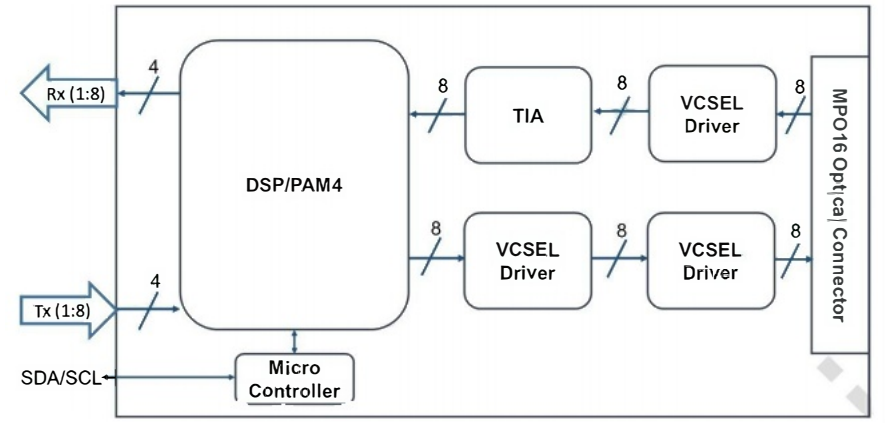


MEMORY MAP (compliant SFF-8636)

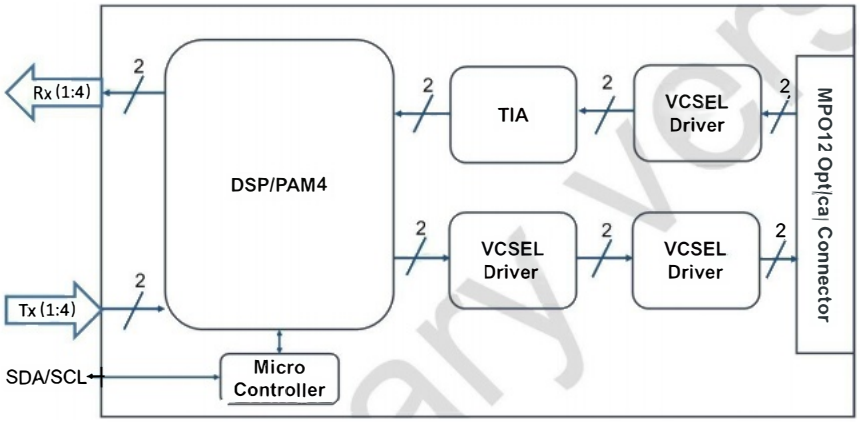
	2-Wire SerialAddress1010000x
	LowerPage00h
0	Identifier
1 - 2	Status
3-21	InterruptFlags
22-23	Free Side Device Monitors
34-81	Channel Monitors
82-85	Reserved
86-98	Control
99	Reserved
100-104	Hardware Interrupt Pin Masks
105-106	Vendor Specific
107	Reserved
108-110	Free Side Device Properties
111-112	Assigned for use by PCI Express
113	FreeSide Device Properties
114-118	Reserve
119-122	Password Change Entry Area(Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte

	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h
128 Identifier	128CC_APPS	128-255 User EEPROM data	128-175 Free Side DeviceThresholds
129-191 Base ID Fields	129 AST Table Length(TL)		
	130-131 Application Code Entry0		
	132-133 Application Code Entry1		
	134-253 other entries		
192-223 Extended ID			176-223 Channel Thresholds
224-255 Vendo rSpecific ID			224 TX EQ & RX Emphasis Magnitude ID
			225 RX output amplitude indicators
			226-241 Channel Monitor Masks
	254-255 Application Code EntryTL		252-255 Reserved

TRANSCEIVER MODULE BLOCK



QSFPDD SIDE



QSFP28 SIDE

Test Center

FS.COM transceivers are tested to ensure connectivity and compatibility in our test center before shipped out. FS.COMtest centerissupported by a variety of mainstream original brand switches and groups of professional staff, helping our customers makethemostefficient use of our products in their systems, network designs and deployments.

The original switches could be found nowhere but at FS.COM test center, eg: Juniper MX960 & EX 4300 series, Cisco Nexus 9396PX&Cisco ASR 9000 Series, HP 5900 Series & HP 5406R ZL2 V3(J9996A), Arista 7050S-64, Brocade ICX7750-26Q & ICX6610-48, AvayaVSP7000MDA 2, etc.

CiscoASR9000Series(A9K-MPA-1X40GE)


ARISTA7050S-64(DCS-7050S-64)

Juniper MX960


Brocade ICX7750-26Q

Extreme Networks X670VVIM-40G4X

Mellanox M3601Q


Dell N4032F

HP5406R ZL2 V3(J9996A)

AVAYA 7024XLS(7002QQ-MDA)

Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COMprovides mustrunthrough programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. Inour test center,we care of every detail from staff to facilities—professionally trained staff, advanced test facilities and comprehensive original-brandswitches, to ensure our customers to receive the optics with superior quality.

Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part

Our in-house coding facility programs all of our partstostandard OEM specs for compatibility on all major vendorsandsystems such as Cisco, Juniper, Brocade, HP, Dell, Aristaandsoon.

With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance

The last test assured step to ensure our products tobeshippedwith perfect package.

Order Information

Type	Data Rate	Length	Form Factor	Voltage(V)	Temp. Range
QDD-400G-4Q4xNAO01	400G/100Gbps	1m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO02	400G/100Gbps	2m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO03	400G/100Gbps	3m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO05	400G/100Gbps	5m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO07	400G/100Gbps	7m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO10	400G/100Gbps	10m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO15	400G/100Gbps	15m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃
QDD-400G-4Q4xNAO20	400G/100Gbps	20m	QSFP-DD to 4x100GQSFP28	3.3	0-70℃