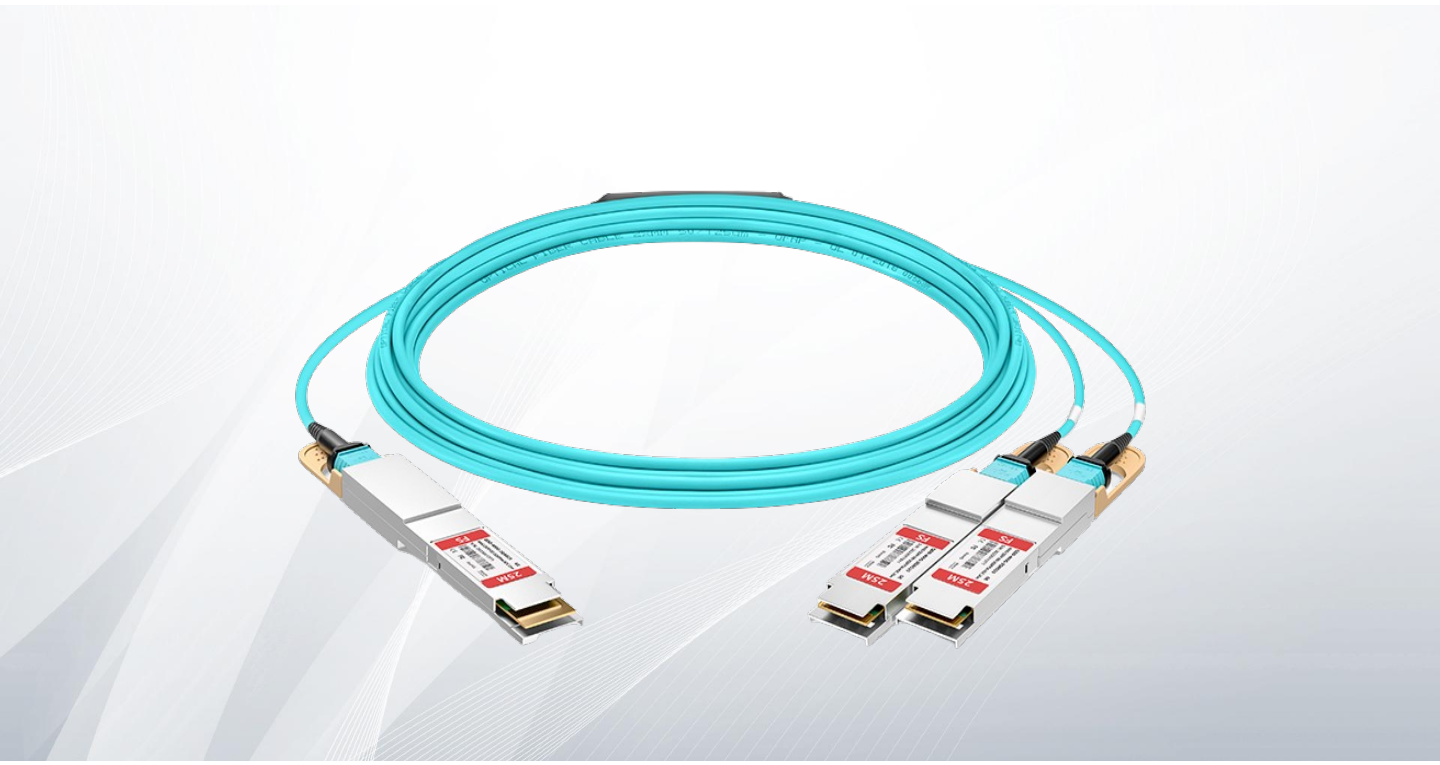
400G QSFP-DD to 2 x200G QSFP56 Active Optical Breakout Cable



Application

- Data Center

Features

- Up to 53.125Gbps Data Rate Per Channel by PAM4 Modulation
- Enable 400G Breakout 2x200G Application
- Support 400GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PIN Array
- Power Dissipation: <4W(200G End) , <8W(400G End)
- Hot Pluggable QSFP-DD and QSFP56 Form Factor
- Maximum Link Length: Up to 30m

Standards

- IEEE 802.3cd, IEEE 802.3bs Annex120E
- OIF-CEI-04.0
- QSFP-DD MSA, QSFP-DD-CMIS-Rev4.0
- SFF-8024 Rev. 4.6, SFF-8679 Rev1.8, SFF-8665 Rev1.9

- Operating Case Temperature Range: 0 to +70°C
- EEPROM in Cable Assembly
- Pre-FEC Max. BER 2.4E-4
- Support RS-FEC
- Single 3.3V Power Supply
- DDM Function Implemented

Description

The FS's 400G QSFP-DD to 2x200G QSFP56 breakout Active Optical Cable operates over Multi-Mode Fiber (MMF). This breakout cable is compliant with IEEE 802.3, QSFP-DD MSA, SFF-8024, SFF-8679, SFF-8665, OIF-CEI-04.0 and CMIS 4.0. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

It provides connectivity between system units with a 400GbE connector on one side and two separate 200GbE connectors on the other side and is suitable for Data Center Appications.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature Range	T_S	-20	85	ºC	
Supply Voltage	V_{CC}	-0.5	4.0	V	
Operating Relative Humidity	RH	0	85	%	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Bit Rate(per Channel)	BR		26.5625		GBd	
Humidity	RH	5		85	%	
Fiber Bend Radius	RB	3			cm	

III. Electrical Specifications

Parameter	Symbol	Units	Min.	Typ.	Max.	Notes
	V_{CC} V_{CC}3.3Tx V_{CC}3.3-Rx	V	3.135	3.3	3.465	
Power Consumption(QSFP-DD)	Pc	W		11		Per-end
Power Consumption(QSFP56)	Pc	W		5		Per-end
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential Peak-to-peak Input Voltage Tolerance		mV	900			
Differential Termination Mismatch					10%	
Differential Input Return Loss(SDD11)		dB			See CEI-56G -VSR	
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD11, SDC11)		dB			See CEI-56G -VSR	
Receiver						
Differential Peak-to-peak Output Voltage		mV			900	
DC Common Mode Voltage	V_{cm}	mV	-350		2850	
AC Common Mode Noise, RMS		mV			17.5	
Differential Termination Mismatch		%			10	
Differential Output Return Loss (SDD22)		dB			See CEI-56G -VSR	
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD22, SDC22)		dB			See CEI-56G -VSR	

Parameter	Symbol	Units	Min.	Typ.	Max.	Notes
IIC Communication						
IIC Clock Frequency(QSFP-DD)		KHZ		400	1000	
IIC Clock Frequency(QSFP56)		KHZ		100	1000	
Clock Stretching		us			500	

IV. Principle Diagram

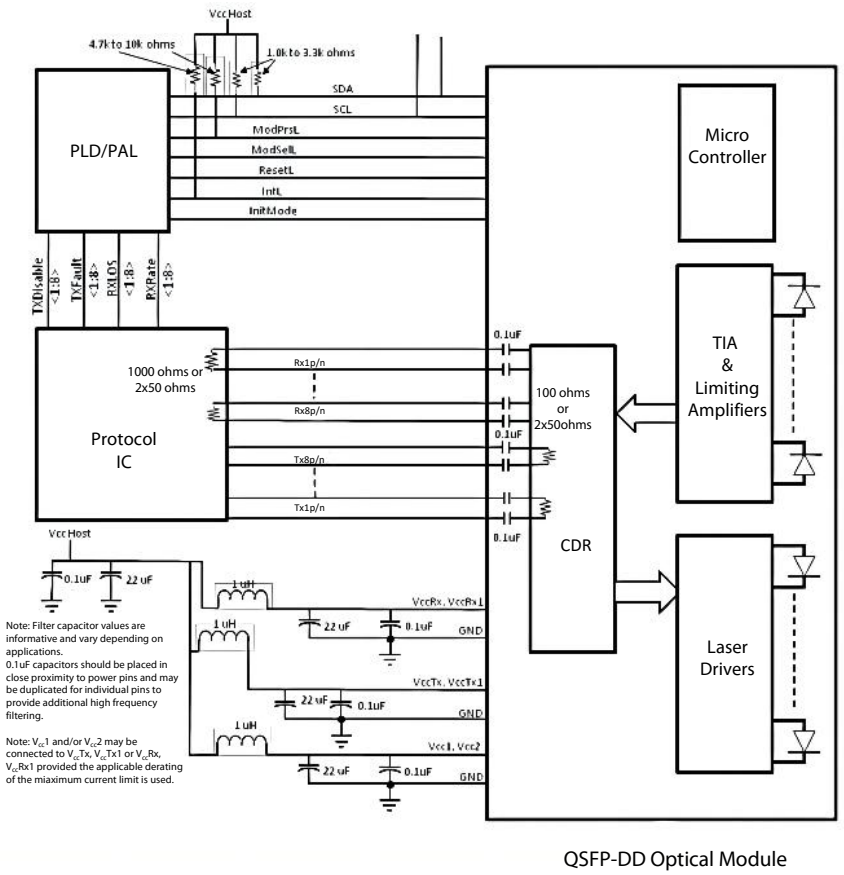


Figure 1. QSFP-DD Principle Diagram

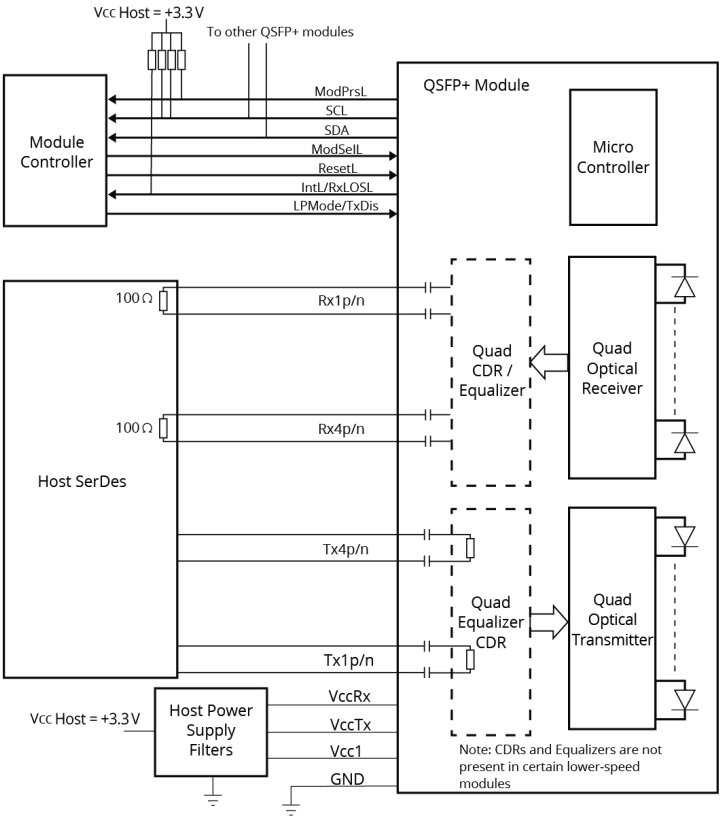
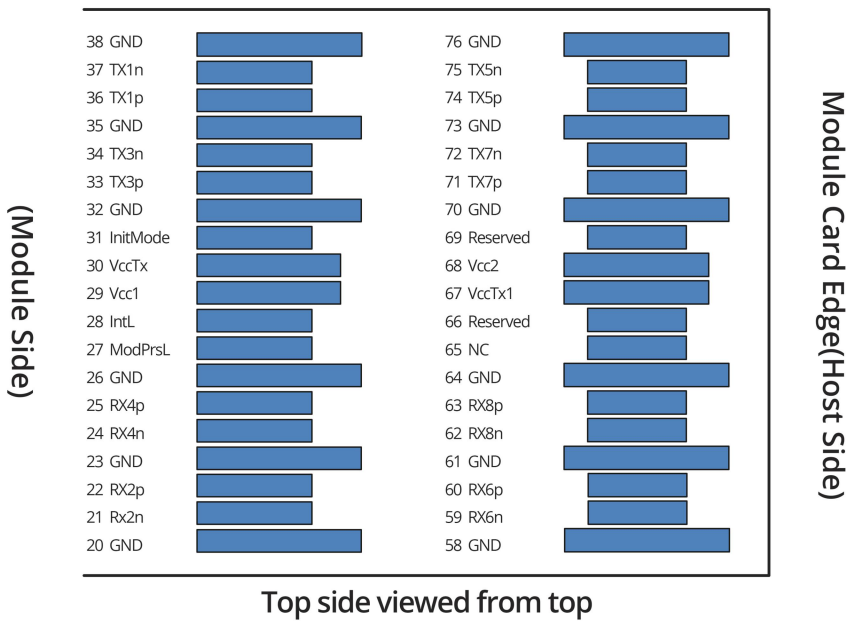
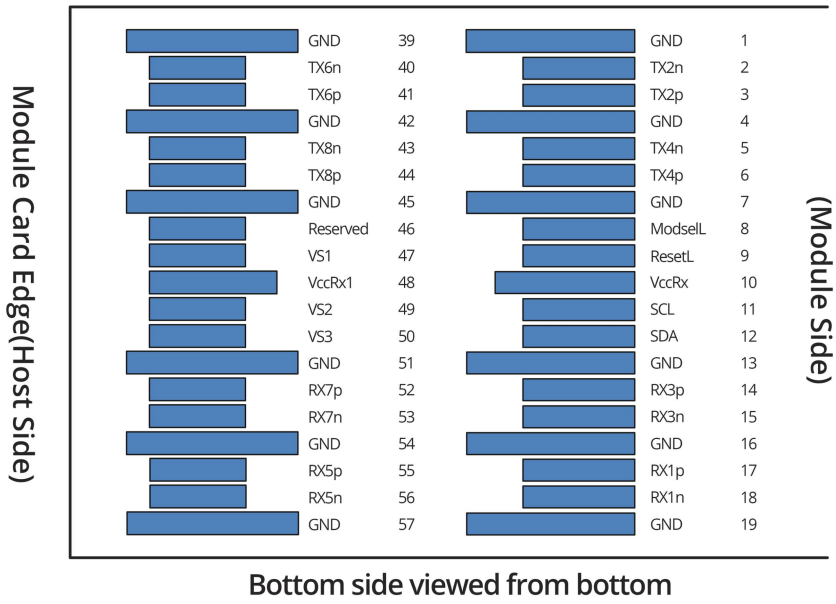


Figure 2. QSFP56 Principle Diagram

V. QSFP-DD Pin Descriptions





Bottom side viewed from bottom

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	

Pin	Logic	Symbol	Description	Note
9	LVTTL-I	ResetL	Module Reset	
10		V_{cc}Rx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	GND	Ground	
18	CML-O	Rx1p	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	

Pin	Logic	Symbol	Description	Note
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		V_{CC}Tx	+3.3 V Power Supply Transmitter	2
30		V_{CC}1	+3.3 V Power Supply	2
31	LVTTL-I	InitMode	Initialization Mode; In Legacy QSFP Applications, the IntiMode Pad Is Called LPMode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	

Pin	Logic	Symbol	Description	Note
45		GND	Ground	1
46		Reserved	For Future Use	3
47		VS1	Module Vendor Specific 1	3
48		V_{CC}Rxx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	

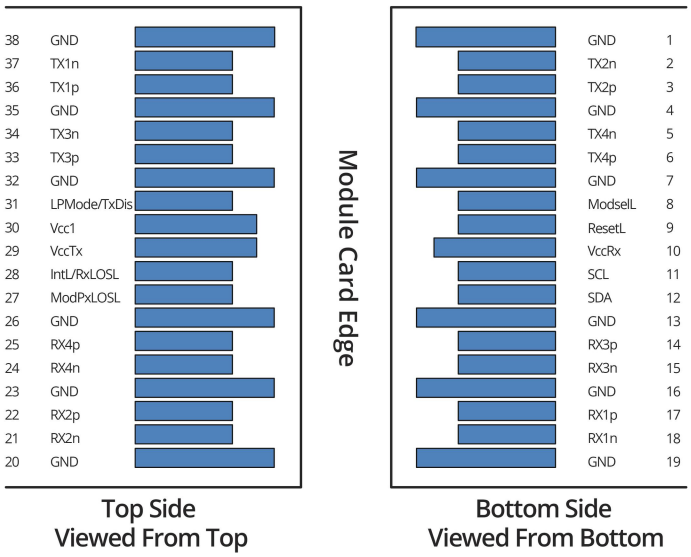
Pin	Logic	Symbol	Description	Note
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For Future Use	3
67		V_{CC}Tx 1	+3.3 V Power Supply Transmitter	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data Output	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data Output	
76		GND	Ground	1

Note 1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

Note 2. V_{CC}Rx, V_{CC}Rx1, V_{CC}1, V_{CC}2, V_{CC}Tx, and V_{CC}Tx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. V_{CC}Rx, V_{CC}Rx1, V_{CC}1, V_{CC}2, V_{CC}Tx, and V_{CC}Tx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

Note 3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.

VI. QSFP56 Pin Descriptions



Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		V_{CC} Rx	+3.3V Power Supply for Receiver	2
11	LVTTL-I/O	SCL	2-wire Serial Interface Clock	

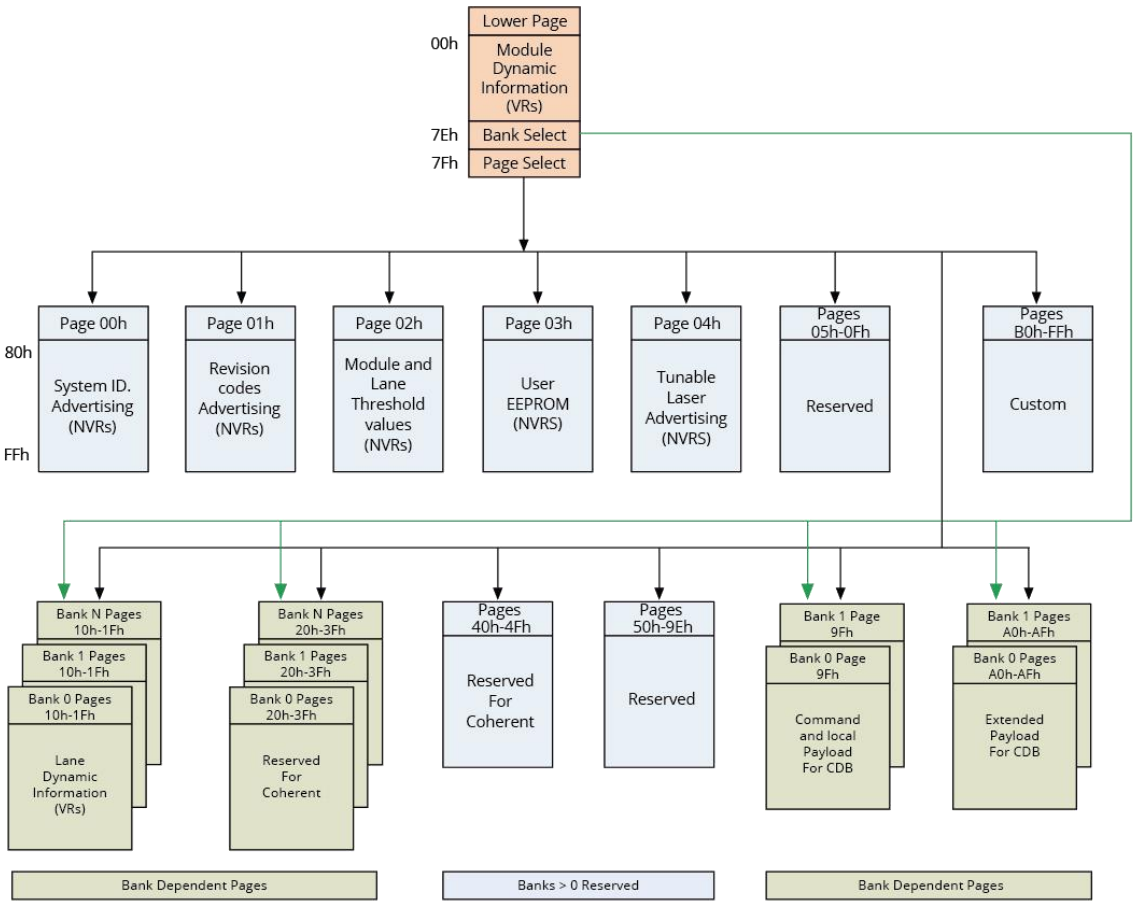
Pin	Logic	Symbol	Description	Notes
12	LVTTL-I/O	SDA	2-wire Serial Interface Data Line	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally Configurable As RxLOSL Via the Management Interface (SFF-8636)	
29		V_{CC} Tx	+3.3v Power Supply For Transmitter	2

Pin	Logic	Symbol	Description	Plug Sequence	Notes
30		$V_{CC}1$	+3.3v Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode. Optionally Configurable As TxDis Via the Management Interface (SFF-8636)	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note2: V_{cc}Rx, V_{cc}1 and V_{cc}Tx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 2 below. V_{cc}Rx, V_{cc}1 and V_{cc}Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

VII. Module Memory Map



VIII. Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

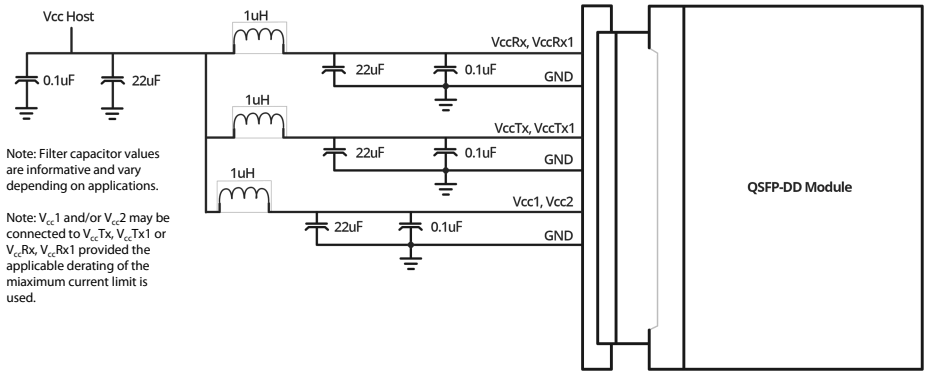


Figure 3. QSFP-DD Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 Ω.The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP+ module Power Classes.Figure is the suggested transceiver/host interface.

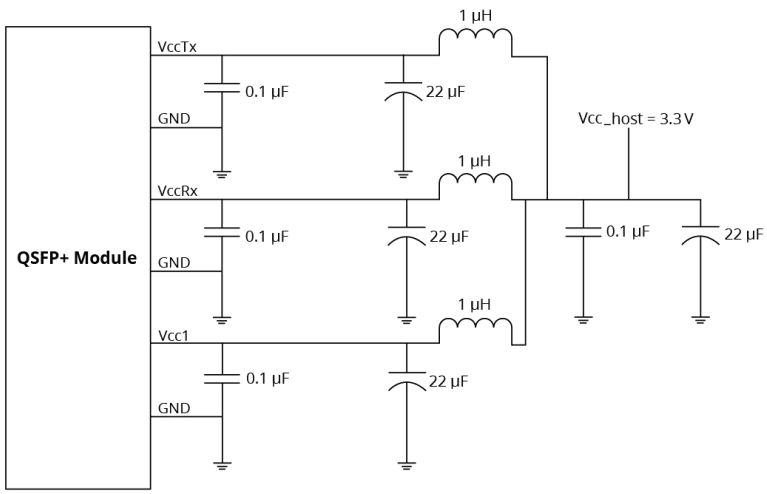


Figure 4. QSFP56 Recommended Host Board Power Supply Filtering

IX. Diagram Mechanial Drawing

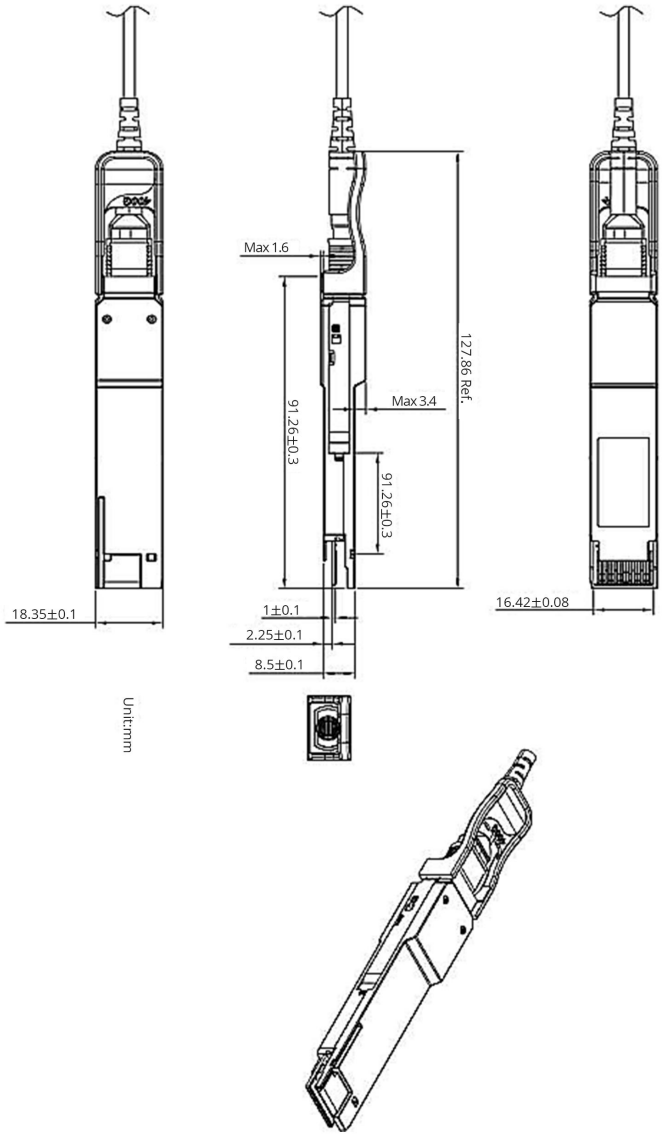


Figure 5. QSFP-DD Diagram Mechanial Drawing

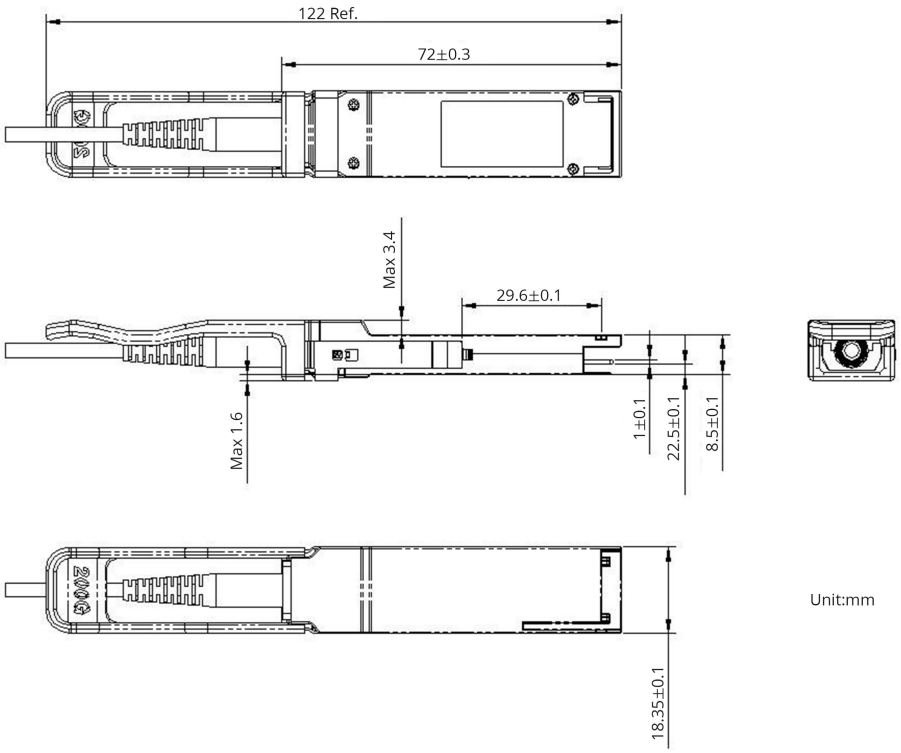


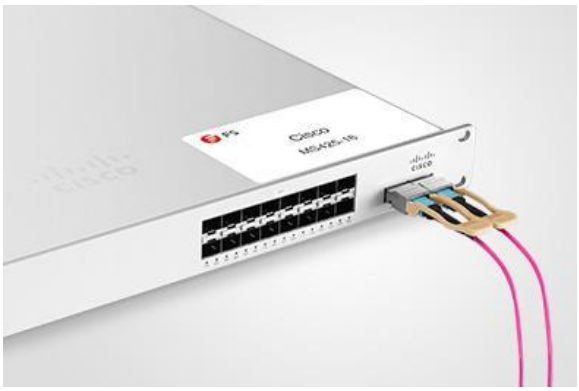
Figure 6. QSFP56 Diagram Mechanial Drawing

Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C



Cisco MS425-16

Brocade VDX 6940-144S

Dell EMC Networking Z9100-ON

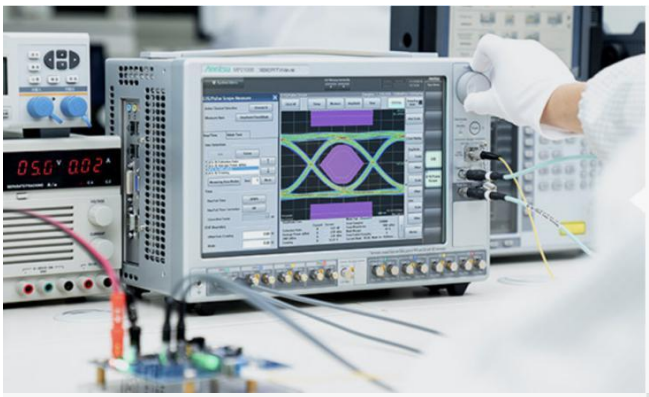
Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C

3. Transfer Rate and Protocol Testing

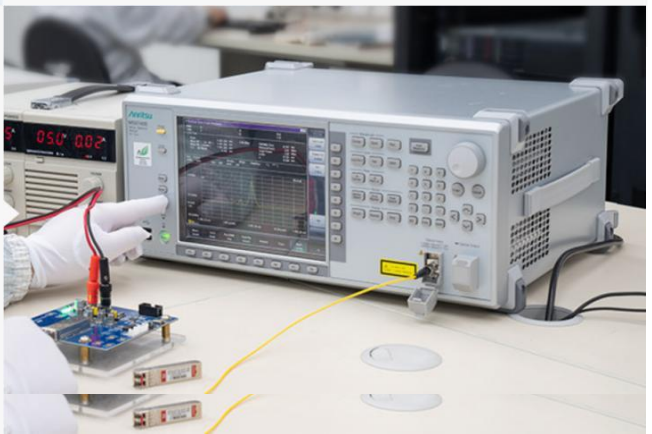
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Data Rate	Length	Connector Type	Temp. Range	Cable Jacket
QDD-400G-2QAO01	Up to 400G	1m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO02	Up to 400G	2m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO03	Up to 400G	3m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO05	Up to 400G	5m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO07	Up to 400G	7m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO10	Up to 400G	10m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO15	Up to 400G	15m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO20	Up to 400G	20m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO25	Up to 400G	25m	AOC Cable	0-70℃	OFNP
QDD-400G-2QAO30	Up to 400G	30m	AOC Cable	0-70℃	OFNP