OSFP-2FR4-1.6T Data Sheet

Application

- 1.6Tbps AI/ML applications and network switch interconnect

Features

- Hot-pluggable OSFP form factor type 2
- 1.6Tbps aggregate bit rate
- Power dissipation <26W
- Case temp range of 0°C to +70°C
- 2000m max on single mode fiber
- Single 3.3V power supply
- 8x 200G PAM4 optics
- 8x 200G PAM4 retimed 212.5GEL PAM4 electrical interface aligned to IEEE 802.3dj
- Back-to-back LC (BBLC) connector
- I2C management interface

Description

The NVIDIA/Mellanox InfiniBand Compatible OSFP Optical Transceiver is an 1.6T 2x 800Gb/s Twin-port OSFP, 2x FR4 single mode, Multiplexed, 8-channel transceiver using two, 2-fiber, LC Duplex optical connectors each carrying 4-channels of 200G-PAM4. The dual far reach 8-channel (2x FR4) design uses 200G-PAM4 electrical and optical modulation based on the CWDM4 serial, multiplexed 1310nm wavelength grid. It is qualified for use in InfiniBand XDR end-to-end systems.

The Closed Finned Top (OSFP-IHS) version is suitable for Quantum-X800 air-cooled and liquid-cooled switches. It is the ideal solution for supercomputing and HPC industries, seamlessly integrating into computing and storage infrastructure to ensure efficient high-performance interconnectivity. The main application is linking two switches together up to 2km.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Maximum Supply Voltage	VCC	-0.5	4.0	V
Storage Temperature	TS	-40	+85	°C
Case Operating Temperature	TOP	0	+70	°C
Relative Humidity (non-condensing)	RH	5	85	%
Receiver Damage Threshold, per Lane	PRdmg	5.9		dBm

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			8.293	A	
Module total power	P			26	W	1

> ⓘ **Notes:** Maximum total power value is specified across the full temperature and voltage range.

III. Optical Characteristics

- **Transmitter**

The transmitter optical specifications are measured at TP2 (module fiber output), with all eight channels active within the voltage and temperature range specified in sections II & III.

Parameter	Min.	Typical	Max.	Unit	Notes
Signaling rate, each lane (range)	106.25± 50 ppm.			GBd	
Modulation format	PAM4				
Lane wavelength	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Side-mode suppression ratio (SMSR), (min)	30			dB	
Average Launch Power, each lane	-2.2		4.9	dBm	1
Outer Optical Modulation Amplitude (OMAouter), Each lane (Max)			4.8	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane (min) **for max(TECQ, TDECQ) <0.9 dB** **for 0.9 dB**	0.8 –0.8 + max(TECQ, TDECQ)			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane			3.4	dB	
| TDECQ - TECQ | , each lane			2.5	dB	
Over/under-shoot (max)			22	%	
Tx power excursion (max)			2.9	dBm	
Extinction ratio, each lane (min)	3.5			dB	
Transmitter transition time (max)			8	ps	
Average launch power of OFF Transmitter, each lane (max)			-16	dBm	
RIN21.4OMA			-139	dBc/Hz	
Optical return loss tolerance (max)			17.1	dB	
Transmitter reflectance (max)			-26	dB	2

- **Receiver**

The receiver optical specifications are measured at TP3 (module fiber input), with all channels active, within the voltage and temperature range specified in sections II & III.

Parameter	Min.	Typical	Max.	Unit	Notes
Signaling rate, each lane (range)		106.25± 50 ppm		GBd	
Modulation format		PAM4			
Lane wavelength(range)	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Damage threshold, each lane		5.9		dBm	3
Average receive power, each lane (max)			4.9	dBm	
Average receive power, each lane (min)	-6.2			dBm	4
Receiver power (OMAouter), each lane (max)			4.8	dBm	
Difference in receive power between any two lanes (OMAouter)			4.1	dB	
Receiver reflectance (max)			-26	dB	
Receiver sensitivity (OMAouter), each lane (max) for TECQ < 0.9 dB for 0.9 dB < TECQ < SECQ			-3.7 -4.6+TECQ	dBm	5
Stressed receiver sensitivity (OMAouter), each lane (max)			-1.2	dBm	5
Conditions of stressed receiver sensitivity test					6
Stressed eye closure for PAM4 (SECQ), lane under test		3.4		dB	
OMAouter of each aggressor lane		0.8		dBm	
Rx LoS de-assert threshold			-9.2	dBm	
Rx LoS Hysteresis	0.5			dB	

ⓘ **Notes:**

Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance. An average launch power of –2.2 dBm corresponds to an OMA of 0.8 dBm with an infinite extinction ratio. An average launch power of –1.1 dBm corresponds to an OMA of 1.9 dBm with an infinite extinction ratio.

Transmitter reflectance is defined looking into the transmitter.

The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Measured with conformance test signal at TP3 (see 183.9.13) for the block error ratio specified in 183.2.

These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

IV. Electrical Characteristics

- **Transmitter**

Parameter	Min.	Typical	Max.	Unit
Signaling rate per lane	106.25± 50 ppm.			Gbd
Single-ended voltage tolerance range	-0.4		1.4	V
DC common-mode voltage tolerance	0.15		1.05	V
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	 0.032 0.08			V
Differential to common mode return loss (min)	Equation (179–27)			dB
Effective return loss	8.5			dB
Differential termination mismatch			10	%
Amplitude tolerance		0.5		
Interference tolerance	Table 176D–10			
Jitter tolerance	Table 176D–11			

- Receiver

Parameter	Min.	Typical	Max.	Unit
Signaling rate per lane	106.5± 50 ppm.			Gbd
Differential peak-to-peak voltage (max) Output disabled Output enabled			 0.03 1	V
DC common-mode voltage tolerance	0.15		1.05	V
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB			 0.015 0.06	V
Effective return loss	8.5			dB
Common-mode to common-mode return loss, *RLcc* (min)	Equation (179–19)			dB
Common-mode to differential-mode return loss, *RLdc* (min)	Equation (179–20)			dB
Transmitter steady-state voltage	0.4		0.5	V
Level separation mismatch ratio *R*LM	0.95			
Linear fit pulse peak ratio	0.567			

Transmitter output waveform **absolute value of step size for all taps** **absolute value of step size for all taps** **value at minimum state for c(–3)** **value at maximum state for c(–2)** **value at minimum state for c(–1)** **value at minimum state for c(0)** **value at minimum state for c(1)**	 0.005 0.12		 0.025 -0.06 -0.34 0.5 -0.2	
Difference signal-to-noise-and distortion ratio, dSNDR (min)	0			dB
Signal-to-residual-intersymbol interference ratio, *SNR*ISI (min)	28			dB
Output jitter (max) **JRMS03** **EOJ03** **J4u03**			 0.023 0.025 0.118	UI

V. Pin Description

The electrical pinout of the OSFP module is shown in Figure 1 below. Signal pin description, its list and electrical to optical lane assignment are shown in tables 1-3.

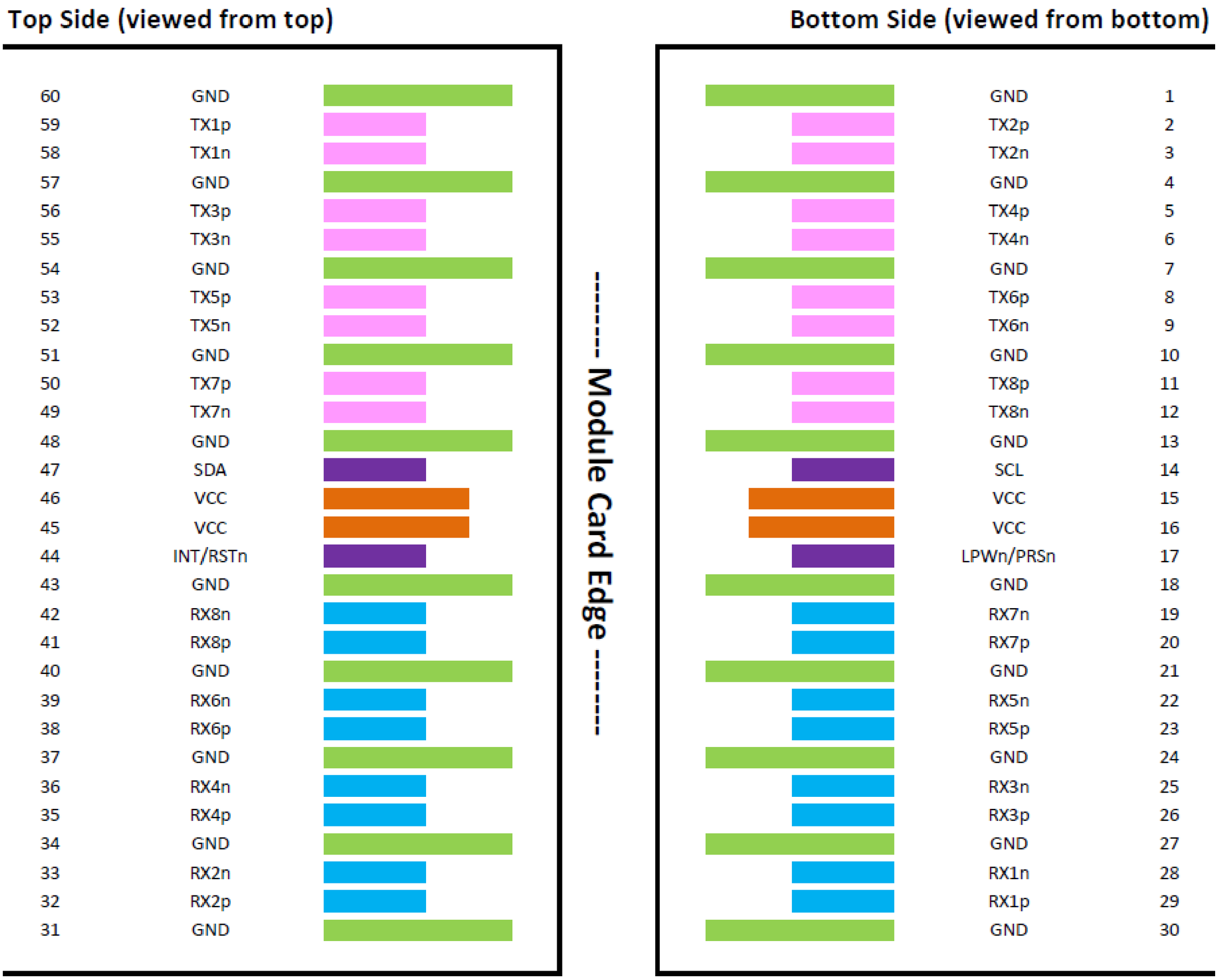


Figure 1 – OSFP Module Pinout (per OSFP MSA)

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 8.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 8.5.2section
VCC	power	3.3V power for module. Each pin provides 1.5 Amps for a total of 6 Amps (19.8 Watts)
GND	ground	Module Ground. Logic and power return path.

Table 1: OSFP Module Signal Pin Descriptions

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

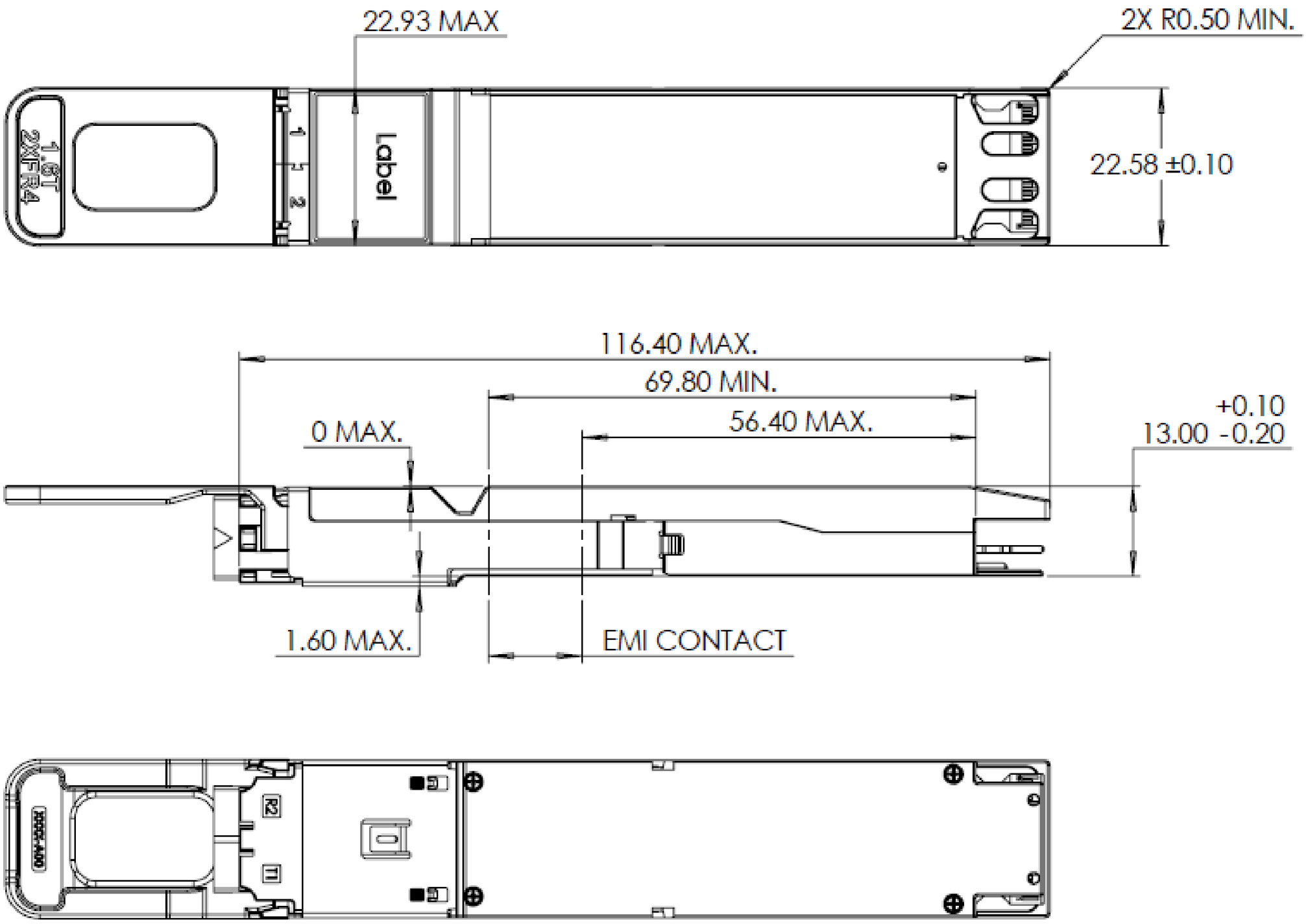
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Table 2-3: OSFP Connector Pin List

VI. Digital Diagnostics

Parameter	Min.	Typical	Max.	Unit
Reported Case temperature accuracy	-3		3	℃
Reported Voltage accuracy	-100		100	mV
Reported Tx output power accuracy	-3		3	dB
Reported Rx input power accuracy	-3		3	dB
Reported Tx bias current accuracy	-10		10	%

VII. Mechanical Dimensions



Shenzhen（China）

Address：Room 1903-1904, Block C, China Resources Tower, Dachong Community, Yuehai Subdistrict, Nanshan District
Email：sales@feisu.com
Tel：+86(400)865 2852

Shanghai（China）

Address：Unit 1201, Lee Gardens Shanghai Office Tower, No. 668 Xinzha Road, Jing'an District
Email：sales@feisu.com
Tel：+86(400)865 2852

Wuhan（China）

Address：Building A1-A4, Chuangxin Tiandi, No. 88 Guanggu Sixth Road, Hongshan District
Email：sales@feisu.com
Tel：+86(400)865 2852