200G/400G DWDM Tunable CFP2 DCO 80km DOM LC SMF Transceiver

CFP2-DCO-400G

Applications

- Designed for line-side trunk DWDM data center interconnect (DCI) and OTU4/OTUCn metro optical transport network.

Features

- Built-in Acacia Chip, Max. Power Consumption 25W
- PM-16QAM (400G/200G), PM-8QAM(300G/200G) and PM-QPSK (200G) Modulation Formats
- Up to 80km over SMF, 1000km (200G) and 200km (400G) with EDFA
- Electrical Interfaces OTL4.4, FOIC1.4, CAUI-4 and FOIC1.2
- Coherent Tunable CFP2 Transceiver, Hot Pluggable

Description

The 400G CFP2-DCO coherent optical module is a high-performance, cost-effective transceiver which uses a 104-pin CFP2-MSA electrical connector for connecting the host card. They are compliant with IEEE802.3bm, OIFCEI-28GVSR, OIFCEI-56GVSRPAM-4.

Product Specifications

I. Performance Specifications

Parameter	Value
200G PM-QPSK Optical Port	
Network Lane, Modulation Format	PM-QPSK
Optical Channels	80
Grid Spacing	75GHz
Frequency Range	190.7 to 196.65THz
Wavelength Stability	±1.5GHz
Tx Output Power, Default	-0.5dBm
Max. Tx Output Power	-0.5dBm
Min. Tx Output Power	-6.5dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±40000ps/nm
Max. Average DGD Tolerance	22ps
Input Power Range	0~18dBm
OSNR Tolerance (BOL)	14.5dB (Rx Optical Power: -8 to -10dBm)
Power Consumption	Typical: 26W Maximum: 28W

Parameter	Value
200G PM-16QAM Optical Port	
Network Lane, Modulation Format	PM-16QAM
Optical Channels	96
Grid Spacing	50GHz
Frequency Range	191.3 to 196.05THz
Wavelength Stability	±1.5GHz
Tx Output Power, Default	-2.5dBm
Max. Tx Output Optical Power	-2.5dBm
Min. Tx Output Power	-6.5dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±40000ps/nm
Max. Average DGD Tolerance	22ps
Input Power Range	0~-18dBm
OSNR Tolerance (BOL)	18.5dB (Rx Optical Power: -8~-10dBm)
Power Consumption	Typical: 22W Maximum: 24W
200G PM-16QAM PS Optical Port	
Network Lane, Modulation Format	PM-16QAM PS
Optical Channels	96

Parameter	Value
Grid Spacing	50GHz
Frequency Range	191.3 to 196.05THz
Wavelength Stability	±1.5GHz
Tx Output Power, Default	-2.5dBm
Max. Tx Output Optical Power	-2.5dBm
Min. Tx Output Power	-6.5dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±40000ps/nm
Max. Average DGD Tolerance	22ps
Input Power Range	0~-18dBm
OSNR Tolerance (BOL)	16.5dB (Rx Optical Power: -8~-10dBm)
Power Consumption	Typical: 22W Maximum: 24W
400G PM-16QAM Optical Port	
Network Lane, Modulation Format	PM-16QAM
Optical Channels	80
Grid Spacing	75GHz
Frequency Range	190.7 to 196.65THz
Wavelength Stability	±1.5GHz

Parameter	Value
Tx Output Power, Default	-2.5dBm
Max. Tx Output Optical Power	-2.5dBm
Min. Tx Output Power	-8dBm
Tx Output Power Accuracy	±1.5dBm
Output Power During Tuning	<-35dBm
CD Tolerance	±15000ps/nm
Max. Average DGD Tolerance	22ps
Input Power Range	0~-18dBm
OSNR Tolerance (BOL)	23 dB (Rx Optical Power: -8~-10dBm)
Power Consumption	Typical: 26W Maximum: 28W

II. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage Temperature	-40	85	℃
Operating Case Temperature	0	70	℃
Relative Humidity, Operating (non-condensing)	5	85	%
Relative Humidity, Operating (Shortterm<96hrs, Non-Condensing)	5	95	%
ESD Sensitivity (HBM)		High-Speed Pins: 1000 Other Pins: 2000	V

III. Electrical Characteristics

1. Power Supply Requirements

1.1 The 400G CFP2-DCO coherent optical module is powered by an independent 3.3 V power supply on the host. All voltages are tested at the connector interfaces.

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
3.3V DC Power Supply Voltage	V_{CC}	3.2	3.3	3.4	V	
3.3V DC Power Supply Current	I_{CC}			8.5	A	Note1 & 2
Power Supply Noise	Vrip			2	%p-p	DC-1MHz
				3		1-10MHz
Power Consumption	Pw_class 4		26	28	W	400G Mode
Operating Temperature	T	0		70	℃	

Note:

1.The Min. and Max. values apply to the full temperature range at the EOL of the module. Typical values (Typ.) are defined at the BOL of the module, with operating temperature at 25℃ and expected power supplied.

2. The maximum current of each pin cannot exceed 1.3 A.

3. The Max. value of Icc is for design reference, and the expected working current cannot exceed Pw_normal/Vcc.

2. High-Speed Electrical Interface Specifications

2.1 The 400G CFP2-DCO coherent optical module provides multiple electrical interfaces.

Client Type	Interface Type	Electrical Standards
100GE	CAUI-4	IEEE 802.3bm CAUI-4, Chip-to-Module
100GE	100GAUI-2	IEEE 802.3bm GAUI-8, Chip-to-Module
200GE	200GAUI-8	OIF CEI-28G VSR
200GE	200GAUI-4	IEEE 802.3bm GAUI-8, Chip-to-Module
400GE	400GAUI-8	
OTU4	OTL4.4	OIFCEI-28G VSR

Client Type	Interface Type	Electrical Standards
OTU4	OTL4.2	OIF CEI-56G VSR PAM-4
OTUC1/OTUC2	FOIC1.4 (FlexO-SR)	OIF CEI-28G VSR
OTUC1/OTUC2/OTUC3/OTUC4	FOIC1.2 (FlexO-SR)	OIF CEI-56G VSR PAM-4

2.2 Reference Clock (REFCLK)

The host does not need to provide a reference clock (REFCLK) for the 400G CFP2-DCO coherent optical module.

2.3 Transmitter Monitor Clock (TXM CLK)

The transmitter of the 400G CFP2-DCO coherent optical module provides a monitoring clock TXMCLK, which is mainly used as a reference for monitoring optical signals at the transmitter. This clock can be used to trigger a high-speed sampling oscilloscope.

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Impedance	Zd	80	100	120	Ω	
Transmitter Monitor Clock FrequencyV(TXMCLK)			1/48		Hz	The Frequency is 1/48 the Symbol Rate of the Transmitter's Optical Signal.
TXMCLK Differential Voltage	V_{DIFFTX}	500		1000	mVppd	Differential Peak-to-peak Voltage

3. Control Pins (non-MDIO) Functional Description

3.1 TX_DIS (Transmitter Disable)

TX_DIS is an input pin which receives signals from the host and operates in the logic high state. When TX_DIS is logic high, the output optical signal inside the optical module is turned off. When TX_DIS is logic low, the output optical signal inside the optical module is turned on.

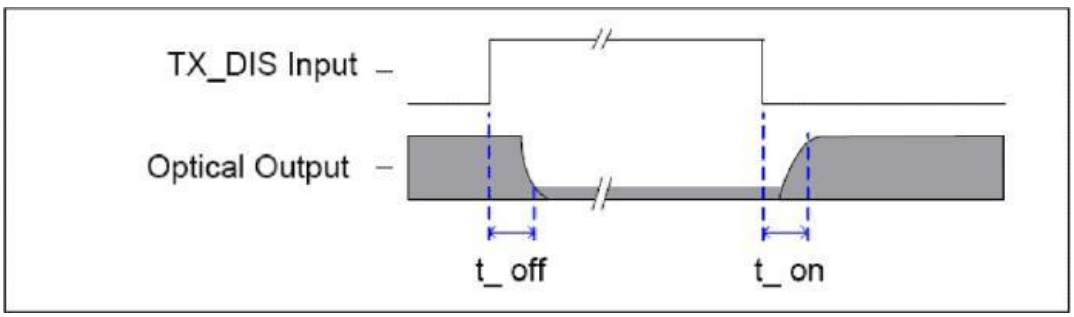


Figure 1. Timing Diagram for TX_DIS

3.2 MOD_LOPWR (Module Low Power)

MOD_LOPWR is an input pin which receives signals from the host and works in the logic high state. When MOD_LOPWR is logic high, the optical module works at low power consumption and remains in this mode. When MOD_LOPWR is pulled down, the optical module is initialized to a high power consumption state, that is, the normal operation mode. In low power consumption mode, the optical module communicates through the MDIO management interface, and its maximum power consumption does not exceed 2 W.

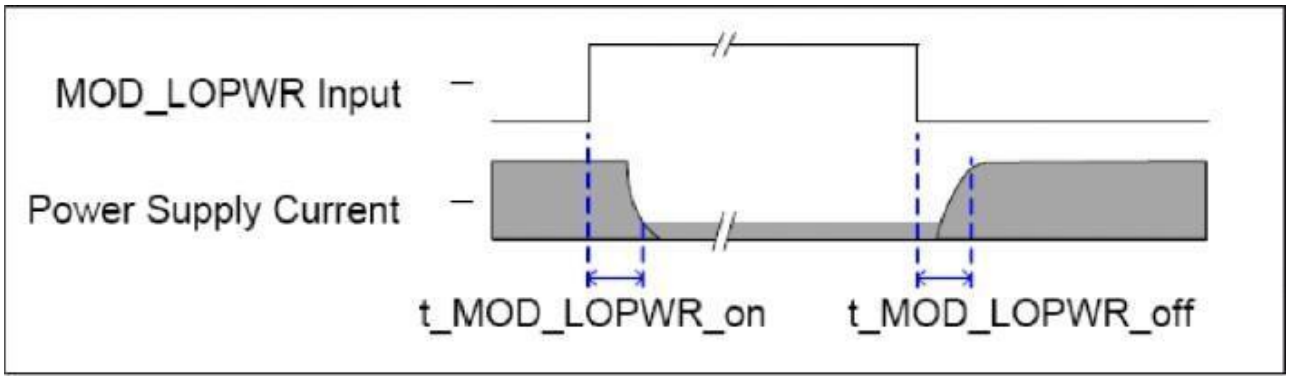


Figure 2.Timing Diagram for MOD_LOPWR

3.3 MOD_ RSTn (Module Reset)

MOD_RSTn is an input pin which receives signals from the host and works in the logic low state. When MOD_RSTn is pulled low, the optical module is in the reset state. When MOD_RSTn is logic high, the optical module exits the reset mode and starts power-on initialization.

4. Alarm Pins (non-MDIO) Functional Description

4.1 RX_LOS (Receiver Loss of Signal)

RX_LOS is an output pin which transmits signals to the host and works at the logic high state. When RX_LOS is logic high, the optical power received by the optical module is too low.

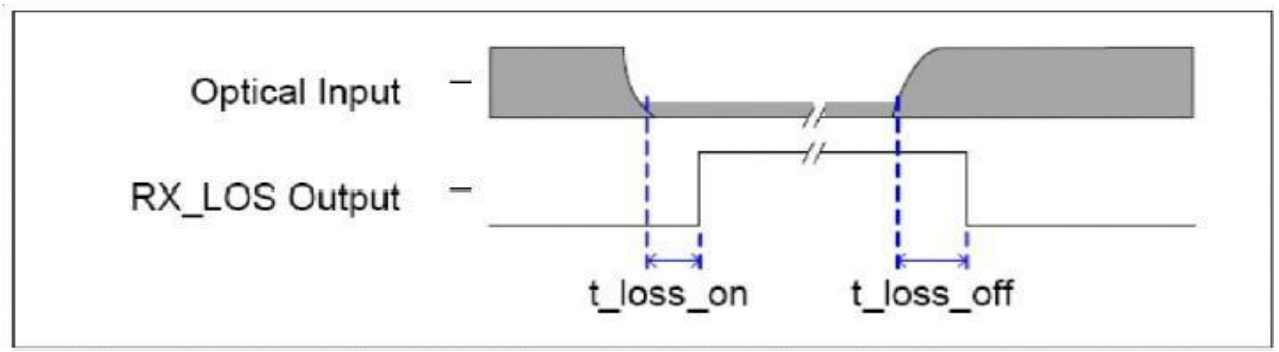


Figure 3.Timing Diagram for RX_LOS

4.2 MOD_ ABS (Module Absent)

MOD_ABS is an output pin which transmits signals from the inside of the module to the host. This pin is pulled up on the host and pulled down to the ground inside the module. When the optical module is inserted into the host, MOD_ABS is logic low, meaning that the module is present. When the optical module is absent on the host, MOD_ABS is logic high, meaning that the module is absent.

5. Control and Alarm Descriptions

5.1 Timing Parameters for Control and Alarm Signals

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter Disabled(TX_DIS high)	t_off			1	ms
Transmitter Enabled(TX_DIS low)	t_on			25	s
MOD_LOPWR assert	t_MOD_LOPWR_assert			25	s

Parameter	Symbol	Min.	Typical	Max.	Unit
MOD_LOPWR deassert	t_MOD_LOPWR_de Assert			25	s
Receiver Loss of Signal Assert Time	t_loss_on			1	ms
Receiver Loss of Signal De-assert Time	t_loss_off			15	ms
Initialization Time From Reset	t_initialize	190		220	s

5.2 3.3V LVCMOS Electrical Characteristics

The 3.3VLVCMO Slevel of the hardware control and alarm signal pins described above shall meet the electrical characteristics. It shows the recommended input and output termination modes for these pins.

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	3.2	3.3	3.4	V
Input High Voltage	VIH	2		V_{CC}+0.3	V
Input Low Voltage	VIL	-0.3		0.8	V
Input Leakage Current	IIN	-10		10	μA
Output High Voltage (IOH=-100μA)	VOH	V_{CC}-0.2			V
Output Low Voltage (IOL=100μA)	VOL			0.2	V

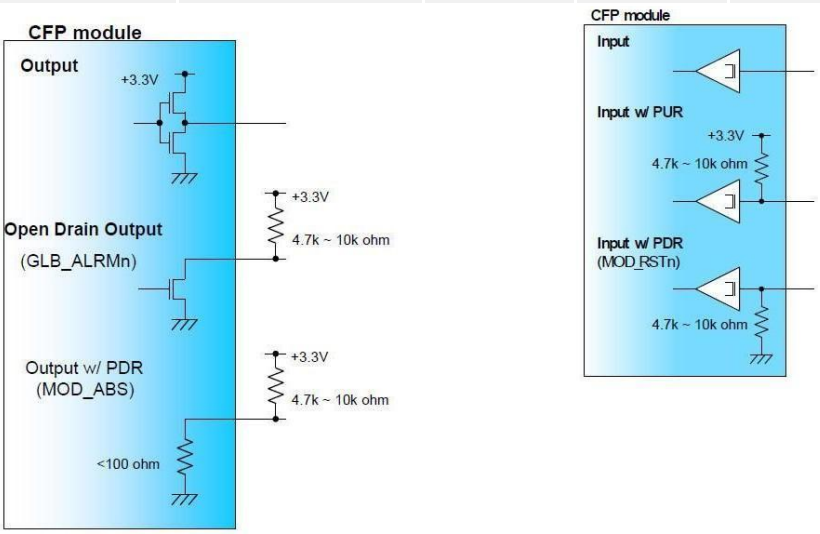


Figure 4.Reference 3.3 V LVCMOS Input / Output Termination

6.Module Management Interface Pins (MDIO) Description

6.1 Management Data Input/Output (MDIO) Interface

The MDIO implementation is defined in IEEE 802.3 clause 45. The MDIO of the optical module uses the 1.2V LVCMOS logic level.

6.2 Management Data Clock (MDC) Interface Pins

The table shows the timing diagram for the MDIO and MDC pins. The optical module should follow the minimum setup time "tsetup" and hold time "thold" requirements of the MDIO port supplementary protocol.

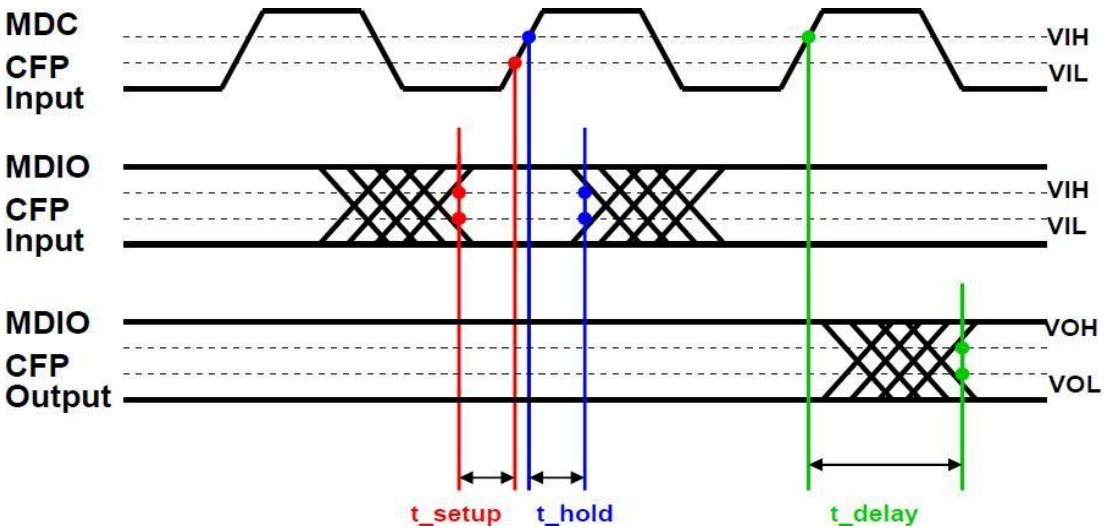


Figure 4. Timing Diagram for the MDIO & MDC Interfaces

Note: Tested on the MDIO & MDC pins of the optical module.

6.3 MDIO Physical Port Address Pins (PRTADRs)

The table shows the timing diagram for the MDIO and MDC pins. The optical module should follow the minimum setup time "tsetup" and hold time "thold" requirements of the MDIO port supplementary protocol.

6.4 1.2VLVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	VIH	0.84	1.5	V
Input Low Voltage	VIL	-0.3	0.36	V
Input Leakage Current	IIN	-100	100	μA
Output High Voltage (IOH=-100μA)	VOH	1	1.5	V
Output Low Voltage (IOL=100μA)	VOL	-0.3	0.2	V
Output High Current	IOH		-4	mA

Parameter	Symbol	Min.	Max.	Unit
Output Low Current	IOL	+4		mA
Input Capacitance	Ci		10	pF

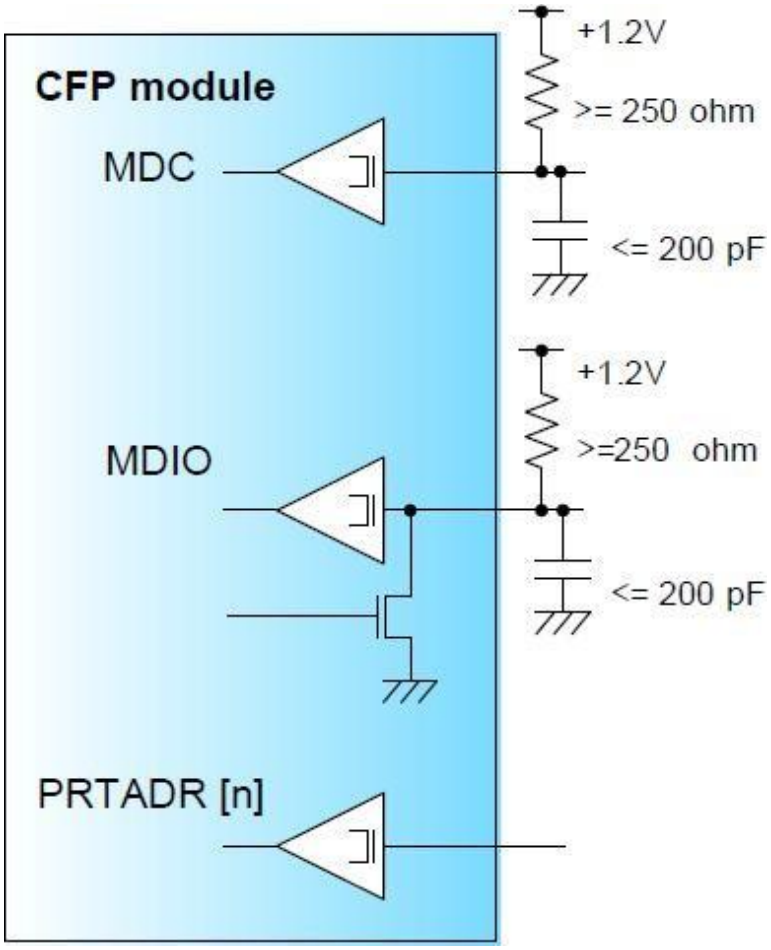


Figure 7.Reference MDIO Interface Termination

IV.Mechanical Specifications

The mechanical dimensions of the 400G CFP2-DCO coherent optical module. Max.dimensions (L×W×H): 107.5mm×42.5mm×13.4mm

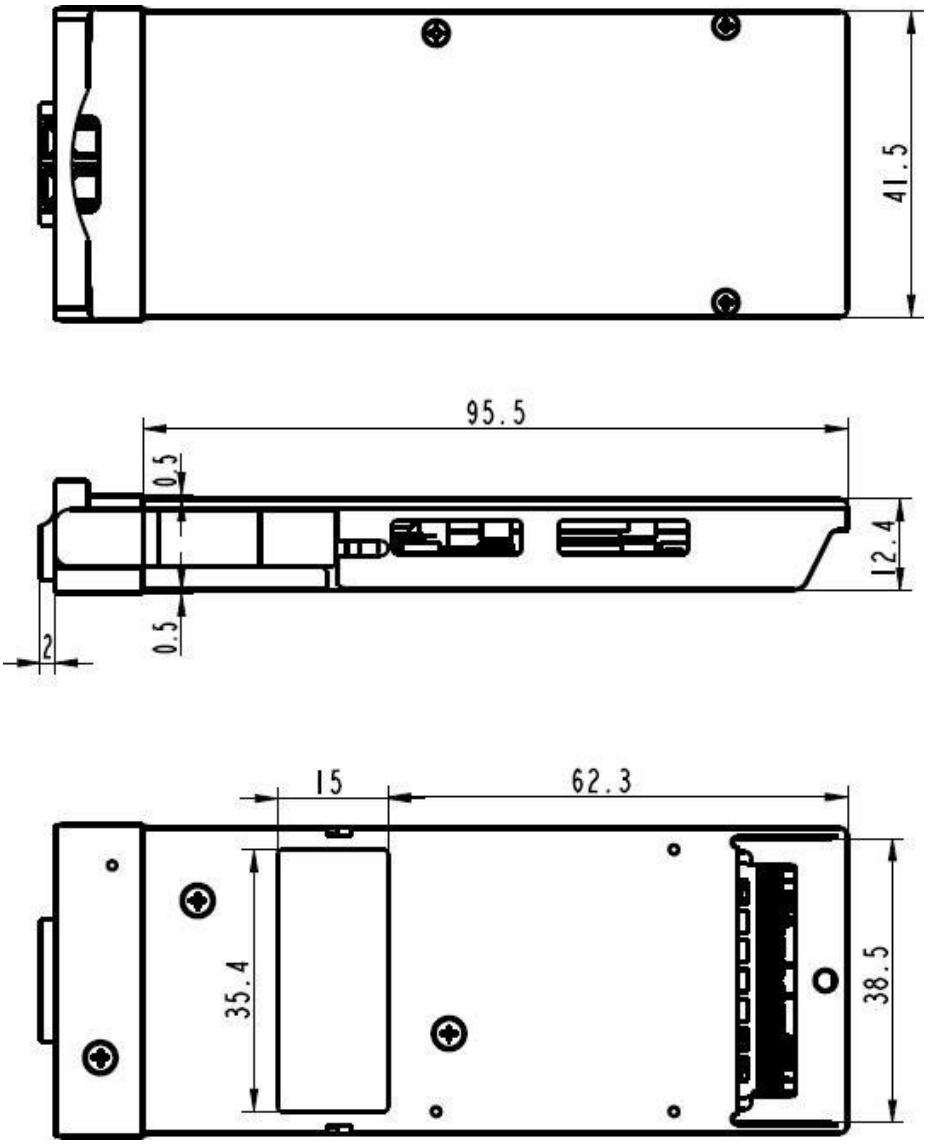


Figure 8. Mechanical Dimensions of the CFP2 Optical Module

V.Pin Description

Pin	Bottom	I/O	Logic	Comment
1	GND	GND	Ground	Module Ground. Logic and Power Return Path
2	OHIO_RDn	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC Coupling Inside Modules
3	OHIO_RDp	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base_X SerDes, AC Coupling Inside Modules
4	GND	GND		Module Ground. Logic and Power Return Path
5	OHIO_TDOn	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC Coupling Inside Modules
6	OHIO_TDOp	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-x SerDes, AC Couping Inside Modules
7	3.3V_GND	GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
8	3.3V_GND	GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
9	33V	PWR		
10	3.3V	PWR		
11	3.3V	PWR		
12	3.3V	PWR		
13	3.3V_GND	GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
14	3.3V_GND	GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
15	VND_IO A	I/O		Customers Must Not Connect to Any of the VND_L10 X Pins Unless Specifially Allowed to do so
16	VND_IO_B	I/O		Customers Must Not Connect to Any of the VND_L10 X Pins Unless Specifially Allowed to do so
17	PRG_CNTL1	I	LVCMOS w/PUR	Internal 10K Pull-up; TRXIC RSTn
18	PRG_CNTL2	I	LVCMOS w/PUR	Internal 10K Pull-up; Hardware Interlock LSB

Pin	Bottom	I/O	Logic	Comment
19	PRG_CNTL3	I	LVCMOS w/PUR	Internal 10k Pull-up; Hardware Interlock MSB
20	PRG_ALRM1	O	LVCMOS	Programmable Aarm 1; MSA Default "H" = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Aarm 2; MSA Default "H" = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 2; MSA Default "H"三MOD. READY
23	GND	GND	Ground	Module Ground. Logic and Power Return Path
24	TX_DIS	|	LVCMOS w/PUR	Transmitter Disabled for all Lanes. Internal 10k Pull-up:
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal; Internal 4.7k Pull-up.
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power; Internal 10k Pull-up;
27	MOD_ABS	O	GND	Module Absent; Internal 50Ω Pull-down;
28	MOD_RSTn	I	LVCMOS w/PDR	Module Reset; Internal 10k Pull-down;
29	GLB_ALRMn	O	LVCMOS	Global Aarm "H" = Alarm; "L" = Ok
30	GND	GND	Ground	Module Ground. Logic and Power Return Path
31	MDC	I	1.2V CMOS	MDIO Clock Input
32	MDIO	I/O	1.2V CMOS	Management Data Input Output.
33	PRTADRO	I	1.2V CMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V CMOS	MDIOPhysical Port Adress bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O		Customers Must Not Connect to Any of the VND_IO-x Pins Unless Specifcallly Allowed to Do So

Pin	Bottom	I/O	Logic	Comment
37	VND_IO_D	I/O		Customers Must Not Connect to Any of the VND_IO-x Pins Unless Specifcallly Allowed to Do So
38	VND_IO_E	I/O		Customers Must Not Connect to Any of the VND_IO-x Pins Unless Specifcallly Allowed to Do So
39	3.3V_GND	GND	Ground	Power Ground. Interally Connected to GND. Logic and Power Return Path.
40	3.3V_GND	GND	Ground	Power Ground. Interally Connected to GND. Logic and Power Return Path.
41	3.3V	PWR		
42	3.3V	PWR		
43	3.3V	PWR		
44	3.3V	PWR		
45	3.3V_GND	GND	Ground	Power Ground. Interally Connected to GND. Logic and Power Return Path.
46	3.3V_GND	GND	Ground	Power Ground. Interally Connected to GND. Logic and Power Return Path.
47	NC	NC	NC	
48	NC	NC	NC	
49	GND	GND	Ground	Module Ground. Logic and Power Return Path
50	TXMONCLKN	O	CML	For Optical Waveform Testing. Not for Normal Use
51	TXMONCLKP	O	CML	For Optical Waveform Testing. Not for Normal Use
52	GND	GND	Ground	Module Ground. Logic and Power Return Path
53	GND	GND	Ground	Module Ground. Logic and Power Return Path
54	RX7p	O	CML	

Pin	Bottom	I/O	Logic	Comment
55	RX7n	O	CML	
56	GND	GND	Ground	Module Ground. Logic and Power Return Path
57	RX0p	O	CML	
58	RX0n	O	CML	
59	GND	GND	Ground	Module Ground. Logic and Power Return Path
60	RX1p	O	CML	
61	RX1n	O	CML	
62	GND	GND	Ground	Module Ground. Logic and Power Return Path
63	RX6p	O	CML	
64	RX6n	O	CML	
65	GND	GND	Ground	Module Ground. Logic and Power Return Path
66	RX5p	O	CML	
67	RX5n	O	CML	
68	GND	GND	Ground	Module Ground. Logic and Power Return Path
69	RX2p	O	CML	
70	RX2n	O	CML	
71	GND	GND	Ground	Module Ground. Logic and Power Return Path
72	RX3p	O	CML	

Pin	Bottom	I/O	Logic	Comment
73	RX3n	O	CML	
74	GND	GND	Ground	Module Ground. Logic and Power Return Path
75	RX4p	O	CML	
76	RX4n	O	CML	
77	GND	GND	Ground	Module Ground. Logic and Power Return Path
78	(REFCLKp)	I	CML	
79	(REFCLKn)	I	CML	
80	GND	GND	Ground	Module Ground. Logic and Power Return Path
81	TX7p	I	CML	
82	TX7n	I	CML	
83	GND	GND	Ground	Module Ground. Logic and Power Return Path
84	TX0p	I	CML	
85	TX0n	I	CML	
86	GND	GND	Ground	Module Ground. Logic and Power Return Path
87	TX1p	I	CML	
88	TX1n	I	CML	
89	GND	GND	Ground	Module Ground. Logic and Power Return Path
90	TX6p	I	CML	

Pin	Bottom	I/O	Logic	Comment
91	TX6n	I	CML	
92	GND	GND	Ground	Module Ground. Logic and Power Return Path
93	TX5p	I	CML	
94	TX5n	I	CML	
95	GND	GND	Ground	Module Ground. Logic and Power Return Path
96	TX2p	I	CML	
97	TX2n	I	CML	
98	GND	GND	Ground	Module Ground. Logic and Power Return Path
99	TX3p	I	CML	
100	TX3n	I	CML	
101	GND	GND	Ground	Module Ground. Logic and Power Return Path
102	TX4p	I	CML	
103	TX4n	I	CML	
104	GND	GND	Ground	Module Ground. Logic and Power Return Path

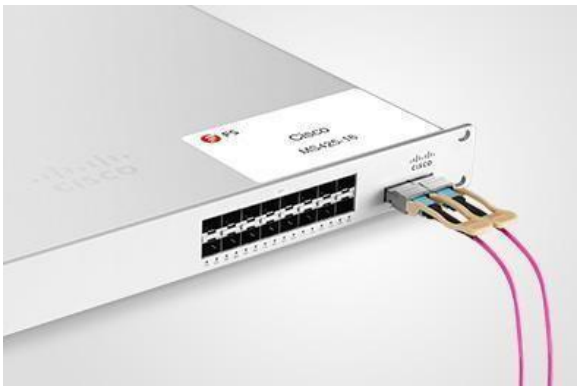
The electrical connection of 104 pin includes eight pairs of TX differential signals (these signals are the input TXI of the module, which connect to the signal outputs of the card), eight pairs of RX differential signals (these signals are the output RXO of the module, which connect to the signal inputs of the card), a pair of monitoring clocks in the Tx direction, control pins, alarm pins, MDIO communication related pins, GND and +3.3V power supply. The +3.3V power supply supports a maximum overcurrent capacity of 1.3A per pin.

Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C



Cisco MS425-16

Brocade VDX6940-144S

Dell EMC Networking Z9100-ON

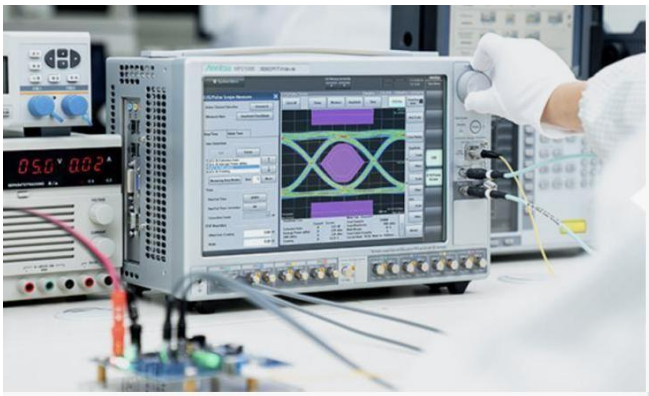
Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C

3. Transfer Rate and Protocol Testing

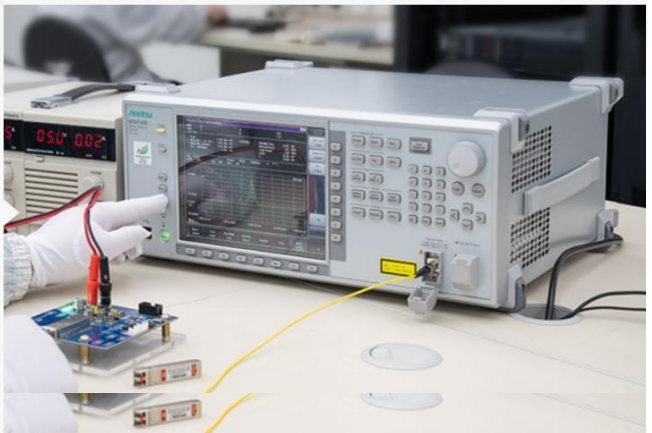
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Ordering Information

Part Number	Description
CFP2-DCO-400G	Generic Compatible CFP2 DCO 200G/400G DWDM Tunable Coherent 80km DOM Duplex LC/UPC SMF Optical Transceiver Module for Transmission