400G QSFP-DD Active Optical Cable

QDD-400G-AOxxx

Application

- 400G BASE-SR8 Ethernet
- Switch & Router Connections
- Data Centers
- Other 400G Interconnect
- Requirements.

Features

- Up to 53. 125Gbps Data Rate per Channel by PAM4 Modulation
- Integrated 850nm VCSEL Array and PD Array
- Support 400GAUI-8 Electrical Interface
- Single +3.3V Power Supply
- DDM Function Implemented
- Hot-pluggable QSFP-DD Form Factor

Low Power Dissipation:≤8.5W

International Class 1 Laser Safety Certified

Operating Temperature Range: 0C ~ +70 C

Compliant with ROHS10

Description

The 400G QSFP-DD SR8 AOC is designed to transmit and receive serial optical data links up to 53. 125 Gb/s data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with the high performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 400G Ethernet specs; QSFP-DD MSA.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max.
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	0	85
Power Supply Voltage	V_{CC}	V	-0.3	+3.465

II. Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ.	Max.
Operating Case Temperature Range	Tc	℃	0	/	70
Power Supply Voltage	V_{CC}	V	3. 135	3.3	3.465
Bit Rate(Per channel)	BR	GBd		26.5625	

III.Electric Ports Definition

Parameter	Symbol	Unit	Min.	Typ.	Max.	Note
Supply Voltage	V_{CC} V_{CC}3.3-Tx V_{CC}3.3-Rx	V	3. 135	3.3	3.465	
Power Consumption	Pc	W			8.5	
Transceiver MgmtInitDuration Time		ms			2000	
Transmitter						
Differential Peak-to-Peak Input Voltage tol		mV	900		10%	
Differential Termination Mismatch		V				
Differential Input Return Loss(SDD11)		dB		IEEE Equation (83E-5)		
Common-Mode to Differential Conversion and Differential to Common-Mode Conversion(SCD11,SDC11)		dB		IEEE Equation (83E-6)		
Stressed Input Test			IEEE 120E.3.4 . 1			
Vcsel Wavelength		nm	840	850	860	
Vcsel Beam Divergence					25°	
Receiver						
Differential Peak-to-Peak Output Voltage		mV			900	
DC Common Mode Voltage	Vcm	mV	-350		2850	
Common Mode Noise, RMS	VcmAC	mV			17.5	

Differential Termination Mismatch		%			10	
Differential Output Return Loss(SDD22)		dB		IEEE Equation (83E-2)		
Common-mode to Differential Conversion and Differential to Common-Mode Conversion(SCD22,SDC22)		dB		IEEE Equation (83E-3)		
Near-End ESMW (Eye Symmetry Mask Width)		UI		0.265		
Near-End Eye Height, Differential		mV		70		
Far-End ESMW (Eye Symmetry Mask Width)		UI		0.2		
Far-End Eye Height, Differential		mV		30		
PD Wavelength		nm	840	850	860	
IIC communication						
IIC Clock Frequency	-	kHZ	/	400	1000	
Clock Stretching	-	us	/	/	500	

IV. Principle diagram

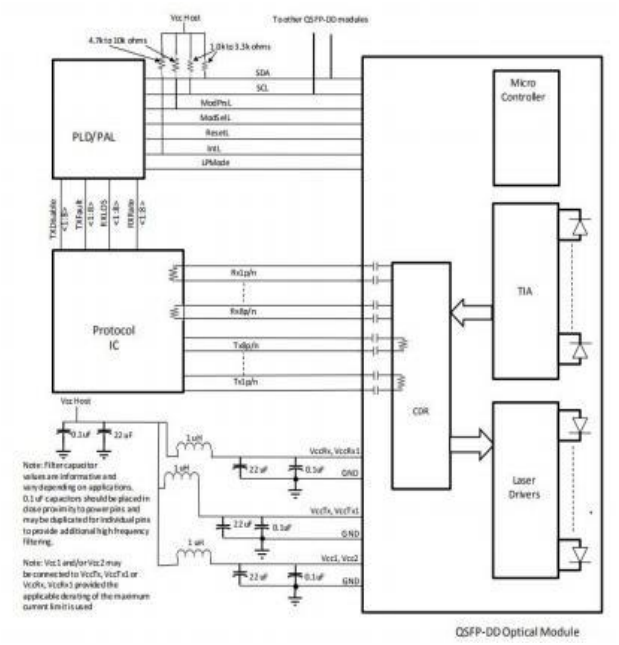


Figure 2. Module Principle Diagram

V. Pin Descriptions

PIN	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	

PIN	Logic	Symbol	Description	Note
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		V_{cc}Rx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx 1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx 1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	

PIN	Logic	Symbol	Description	Note
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	ModPrsL	Module Present	
28	LVTTL-0	IntL	Interrupt	
29		V_{cc}Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data output	
35		GND	Ground	1
36	CML-I	Tx 1p	Transmitter Inverted Data Input	
37	CML-I	Tx 1n	Transmitter Non-Inverted Data output	
38		GND	Ground	1

PIN	Logic	Symbol	Description	Note
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data output	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		V_{cc}Rx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1

PIN	Logic	Symbol	Description	Note
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		V_{cc}Tx 1	+3.3 V Power Supply transmitter	2
68		V_{cc}2	+3.3 V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1

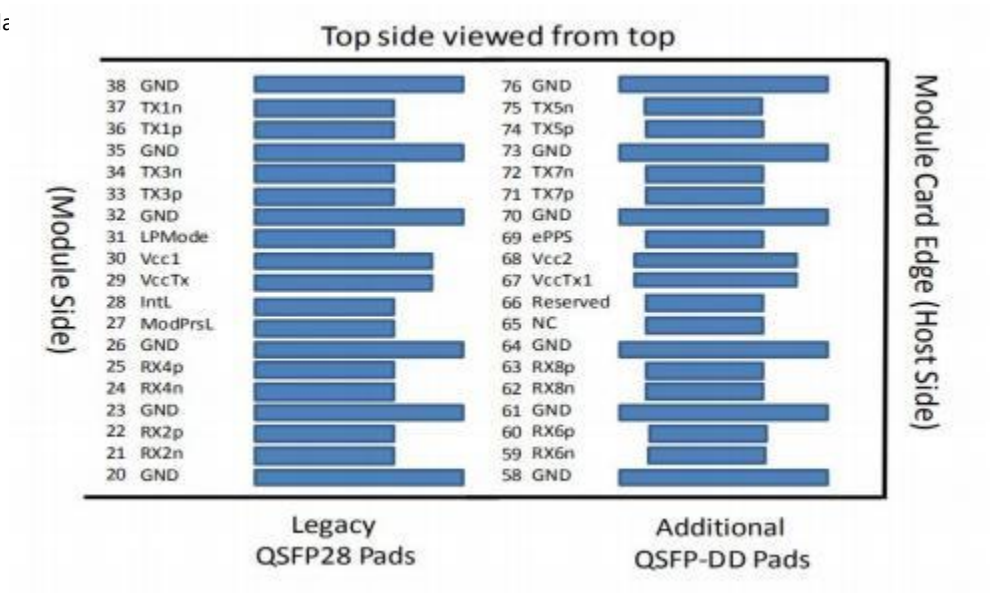
PIN	Logic	Symbol	Description	Note
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data output	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data output	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

2. VccRx, VccRx 1, Vcc1, Vcc2, VccTx, and VccTx 1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx 1, Vcc1, Vcc2, VccTx, and VccTx 1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impeda



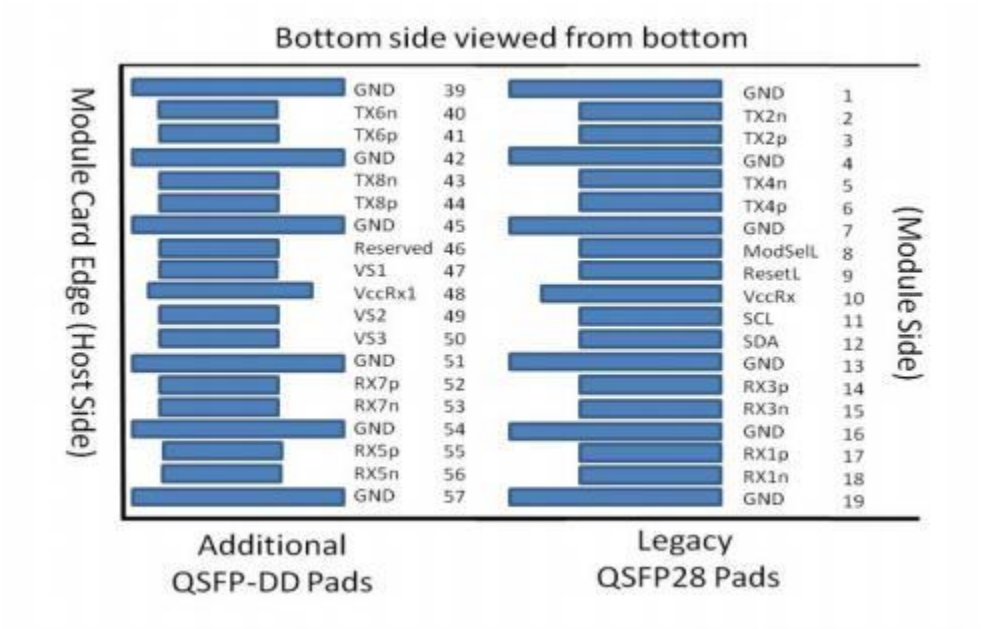


Figure 3. Electrical Pin-out Details

VI. Module Memory Map

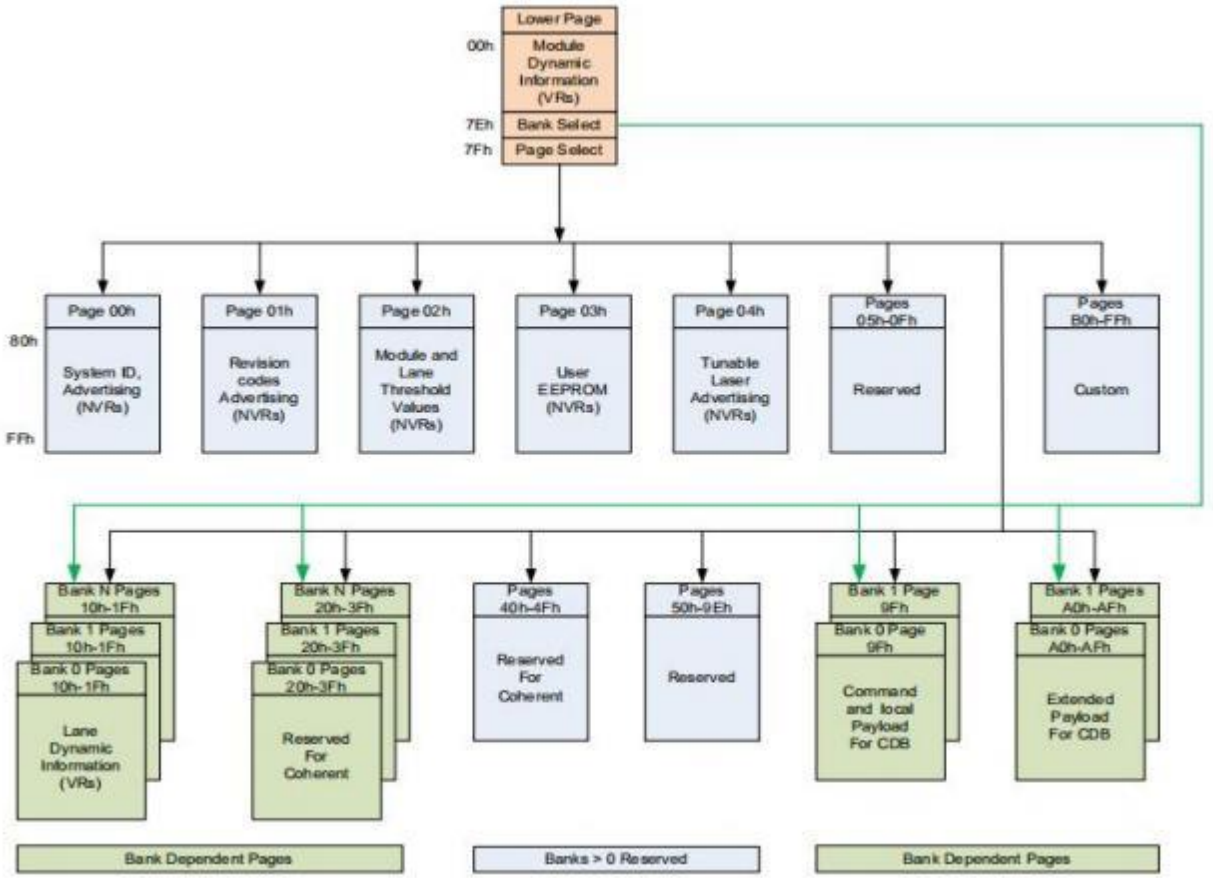


Figure 4 Digital Diagnostic Memory Map

VII. Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0. 1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

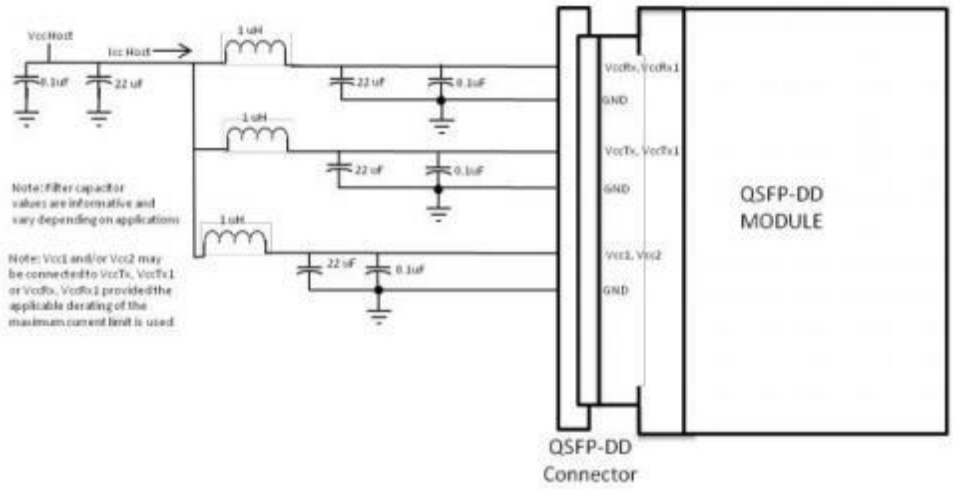


Figure 5 Recommended Host Board Power Supply Filtering

VIII. Package Outline

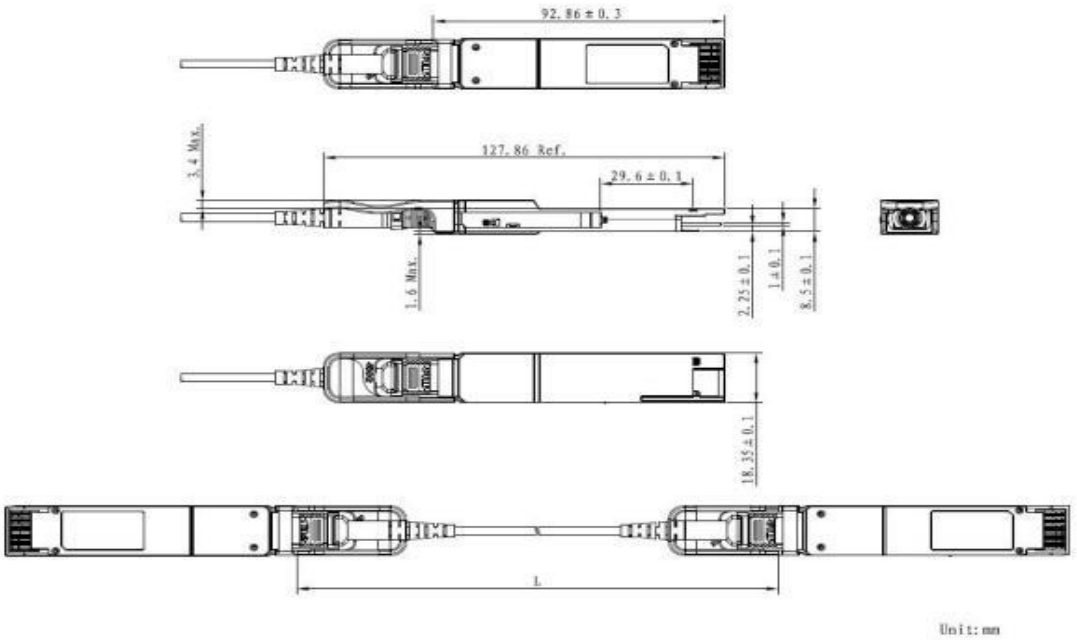


Figure 6 Package Outline

Document History

Ver. & Status	Date	Description of Change	Modifier
V1.0	2023-3-30	Preliminary-Atlas HP	SHJ

Order Information

Part No.	Product	Electrical Mode	Nominal Rate			Specifications		Link
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER	
QDD-400G-AO100	QSFP-DD-400G-AOC 100M	8X53. 125Gbps	425	26.5625 PAM4	± 100	400GAUI- 8	2.4E-4	Customized