800G QSFP-DD Active Optical Cable

QDD-800G-AOxxx

Overview

The 800G QSFP-DD Active Optical Cable is designed for 800 Gigabit Ethernet links over OM4 multimode fiber. This cable is compliant with IEEE 802.3ck, QSFP-DD HW Specification Rev 6.3, and CMIS Rev 5.0. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

It provides a cost-efficient solution as compared to using discrete optical transceivers and optical patch cables and is suitable for 800G connections within racks and across adjacent racks.

Features

- Max. Power Consumption 12W
- Hot-Pluggable QSFP-DD MSA Compliant
- Support 0.5m~50m Transmission with OM4 MMF
- VCSEL Rransmitter and PIN PD Receiver
- Case Operating Temperature 0°C to 70°C
- Two Wire Serial Interface with DDM
- Compliant with IEEE 802.3ck
- Compliant with CMIS Rev 5.0
- Class 1 Laser Safety and RoHS Compliant

Product Specifications

I . Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	85	%
Data Input Voltage Differential	|VDIP-VDIN|	-	1	V
Control Input Voltage	VI	-0.3	Vcc+0.5	%
Control Output Current	Io	-20	20	mA

II . Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	°C	1
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC IP	-	-	TBD	mA	
Sustained Peak Current at Hot Plug	ICC SP	-	-	TBD	mA	
Maximum Power Dissipation	PD	-	-	TBD	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	VIH	Vcc*0.7	-	Vcc+0.3	V	
Control Input Voltage Low	VIL	-0.3	-	Vcc*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
BER	-	-	-	2E-4	-	Pre-FEC

Functional Characteristics (Electrical)

III. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Receiver (Module Output, TP4)						
Signaling rate, each lane (range)	-		53.125 ± 100 ppm		GBd	
Peak-to-peak AC Common-mode Voltage	-				mV	
Low-frequency, VCMLF Full-band, VCMFB		-	-	32 80		
Differential Peak-to-peak Output Voltage	-					
Short Mode Long Mode		-	-	600 845	mV	
Eye Height	EH	15	-	-	mV	
Vertical Eye Closure	VEC	-	-	12	dB	
Common-mode to Differential-mode Return Loss	RLDc		802.3ck 120G-1		dB	
Effective Return Loss	ERL	8.5	-	-	dB	
Differential Termination Mismatch	-	-	-	10	%	
Transition Time	-	8.5	-	-	ps	
DC common-mode Voltage Tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Signaling Rate, each lane (range)	-		53.125 ± 100 ppm		GBd	
Differential pk-pk Input Voltage Tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC Common-mode Voltage Tolerance	-				mV	
Low-frequency, VCMLF		-	-	32		
Full-band, VCMFB				80		
Differential-mode to Common-modeReturn Loss	RL_{cd}		802.3ck 120G-2		dB	
Effective Return Loss	ERL	8.5	-	-	dB	
Differential Termination Mismatch	-	-	-	10	%	
Single-ended Voltage Tolerance Range	-	-0.4	-	3.3	V	
DC Common-mode Voltage Tolerance	-	-0.35	-	2.85	V	

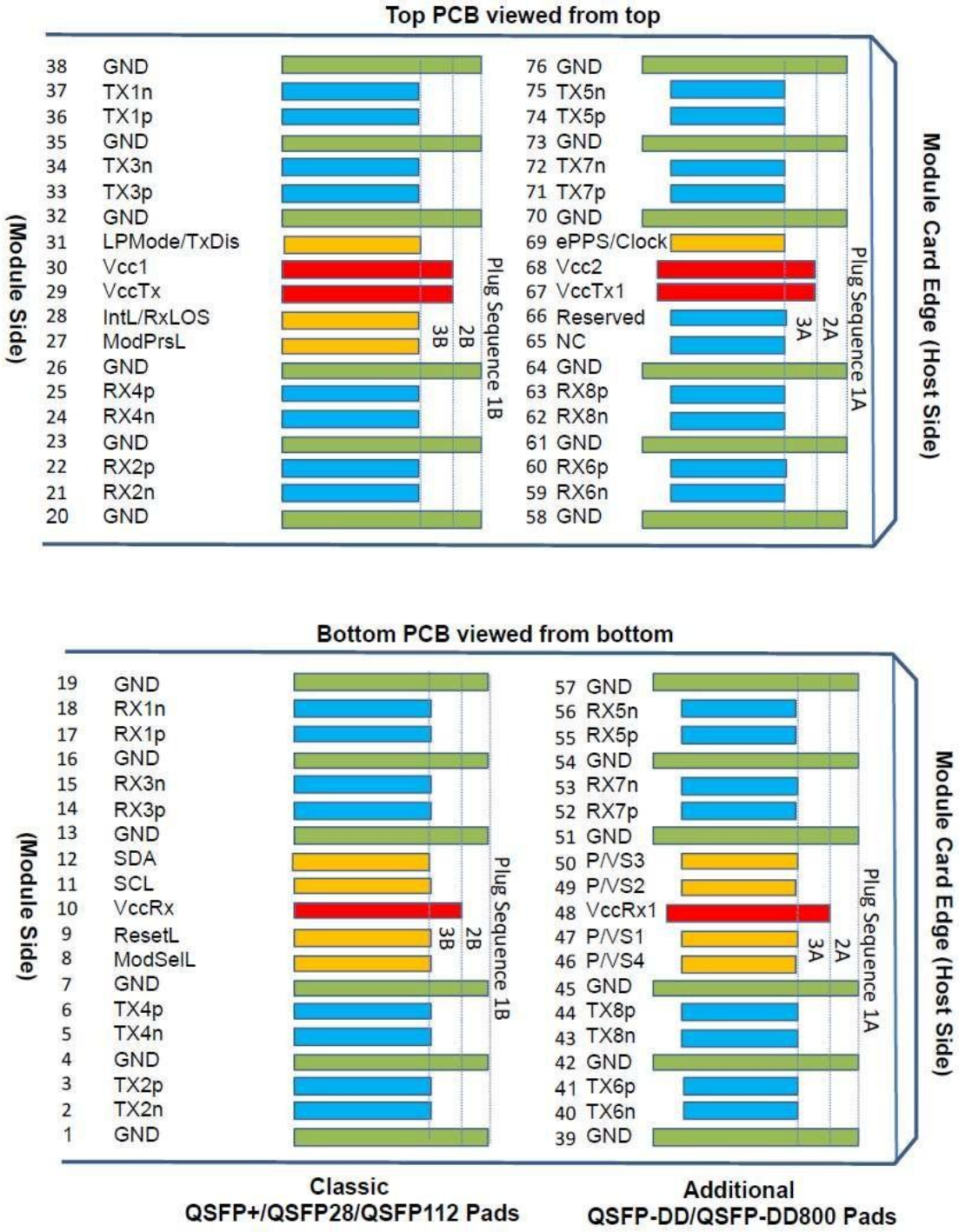
IV. Electrical Specification Low Speed Control and Sense Signals

(Compliant with QSFP-DD HW Rev 6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
Module output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	Vcc*0.3	V
	V_{IH}	Vcc*0.7	Vcc+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	Vcc+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	Vcc-0.5	Vcc+0.3	V

V. Pin Definitions

Figure 1 – Pin definitions of the module high speed inputs/outputs



VI. Module Pin Definitions

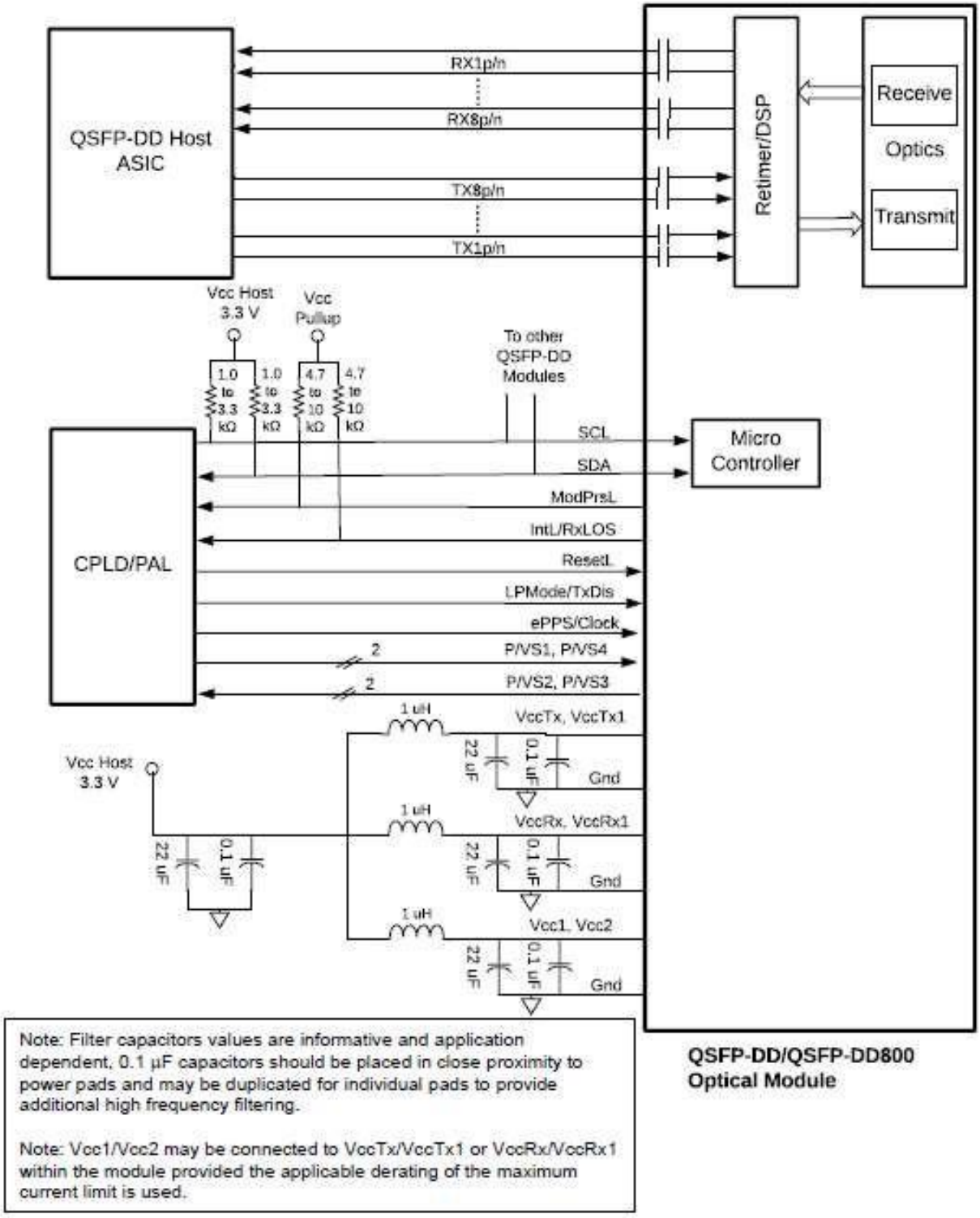
Pin #	Logic	Symbol	Definition
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS -I/O	SCL	TWI serial interface clock
12	LVCMOS -I/O	SDA	TWI serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output

Pin #	Logic	Symbol	Definition
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVCMOS/CML- I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCMOS/CML- I	P/VS1	Programmable/Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3

Pin #	Logic	Symbol	Definition
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not connected
66		Reserved	
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69	LVCMOS-I	ePPS/Cloc k	1PPS PTP clock or reference clock input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7N	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5N	Transmitter Inverted Data Input
76		GND	Ground

VII. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

Figure 2 – Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



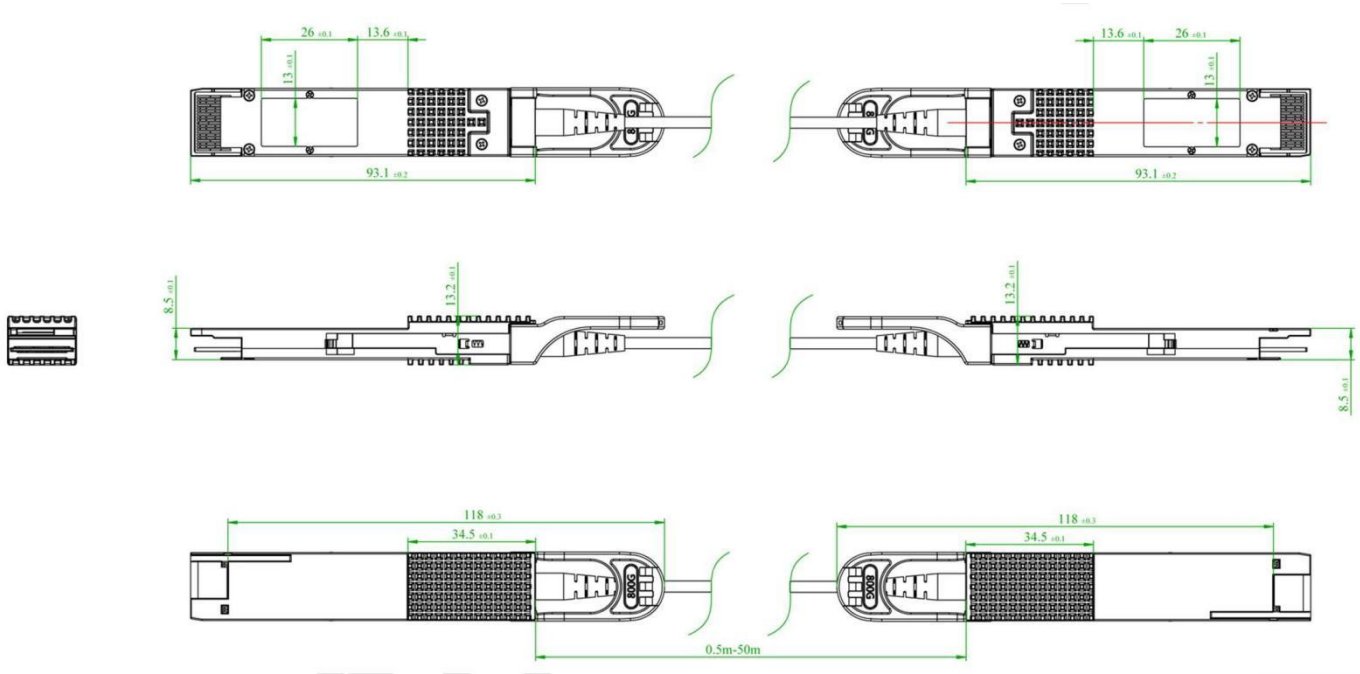
Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

VIII. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	0.1	V	Internal

Mechanical Diagram



Order Information

Part Number	Data Rate	Length	Laser Source	Fiber Type	Temp. Range
QDD-800G-AO01	800G	1m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO02	800G	2m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO03	800G	3m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO05	800G	5m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO07	800G	7m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO10	800G	10m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO15	800G	15m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO20	800G	20m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO30	800G	30m	VCSEL	Multi-Mode Fiber	0°C to 70°C
QDD-800G-AO50	800G	50m	VCSEL	Multi-Mode Fiber	0°C to 70°C