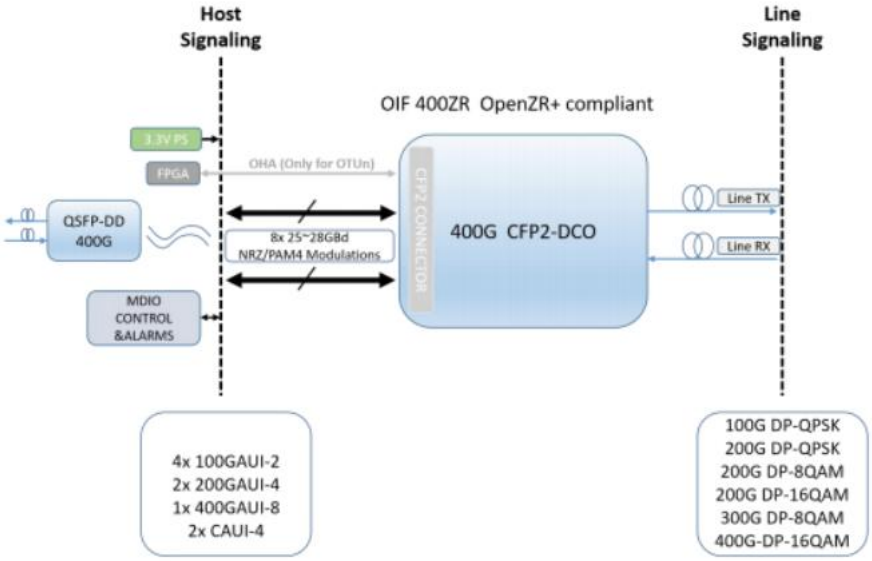
CFP2-DCO-400G-D
Data Sheet

Contents

Descprition

CFP2-DCO-400G-D is CFP2 form factor coherent pluggable module compliant to the CFP MSA CFP2 hardware specification, based on DP-mQAM modulation, polarization diversity coherent intradyne detection and advanced electronic link equalization. On the host side, the module can accommodate a variety of signal types including 4x 100GE,2x 200GE, 1x 400GE, OTUCn(n=[1..4]), and OTU4. On the line side, the module supports 100G, 200G, 300G, and 400G interfaces with different modulation formats and forward error correction (FEC) codes Multiple 100G clients can be multiplexed onto a single 200G, 300G, or 400G line side interface. The module support LLDP function.



Operation Mode

CFP2-DCO-400G-D family operates as either an Ethernet/OTN transceiver/Transponder or an Muxceiver/Muxponder aggregates up to 4x 100G or 2x 200G at the Host/Client interface up to its configured line-side optical capacity.

Table 1. Line-side Mode

Line	Framing	FEC	Symbol Rate (GBaud)	Short Name
100G QPSK	100ZR+	OFEC	30.07	100G 100ZR-OFEC-QPSK
100G QPSK	FLEXO-1	OFEC	31.57	100G FOIC1-OFEC-QPSK
200G QPSK	200ZR+	OFEC	60.14	200G 200ZR-OFEC-QPSK
200G 8QAM	200ZR+	OFEC	40.09	200G 200ZR-OFEC-8QAM

Table 1. Line-side Mode

Line	Framing	FEC	Symbol Rate (GBaud)	Short Name
200G 8QAM	200ZR+	OFEC	40.09	200G 200ZR-OFEC-8QAM
200G 16QAM	200ZR+	OFEC	30.07	200G 200ZR-OFEC-16QAM
200G QPSK	FLEXO-2	OFEC	63.14	200G FOIC2-OFEC-QPSK
200G 8QAM	FLEXO-2	OFEC	42.09	200G FOIC2-OFEC-8QAM
200G 16QAM	FLEXO-2	OFEC	31.57	200G FOIC2-OFEC-16QAM
300G 8QAM	300ZR+	OFEC	60.14	300G 300ZR-OFEC-8QAM
300G8QAM	FLEXO-3	OFEC	63.14	300G FOIC3-OFEC-8QAM
400G 16QAM	400ZR	CFEC	59.84	400G 400ZR-CFEC-16QAM
400G 16QAM	400ZR+	OFEC	60.14	400G 400ZR-OFEC-16QAM
400G 16QAM	FLEXO-4	OFEC	63.14	400G FOIC4-OFEC-16QAM

Table 2. Host-side Mode

Protocol	Interface	Rate GBaud Per Lane	Signaling and Termination	PCS FEC	Reference Standard(s)
Ethernet	1x 400GAUI-8 2x 200GAUI-4 4x 100GAUI-2	26.562500 (+/-100ppm)	PAM-4 Signaling, Internally Terminated, and AC Coupled	RS-FEC (544,514)	IEEE 802.3TM-2018 Clause 91, 119 IEEE 802.3TM-2018 Annex 120E (C2M)
	2x CAUI-4 w/FEC	25.781250 (+/-100ppm)	NRZ Signaling, Internally Terminated, and AC Coupled	RS-FEC (528,514)	IEEE 802.3TM-2018, Clause 83D, 93, 91, and Annex 83E (C2M)
	2x CAUI-4			None	
OTUCn (n=[1..4])	1x FOIC4.8-RS	27.952369 (+/-20ppm)	PAM-4 Signaling, Internally Terminated, and AC Coupled	RS-FEC (544,514)	ITU-T G.709.1 Y.133.1 ITU-T G.Sup58 (10/2018) IEEE 802.3TM-2018 Clause 91, 119
	2x FOIC2 4-RS				
	4x FOIC1.2-RS				
	2x OTLC.4	28.076177 (+/-20ppm)	NRZ Signaling, Internally Terminated, and AC Coupled	GFEC (255,239)	ITU-T G.Sup58 (10/2018) OIF-CEI-04.0 CEI-28G-VSR Very Short Reach Interface - Clause 13

Table 2. Host-side Mode

Protocol	Interface	Rate GBaud Per Lane	Signaling and Termination	PCS FEC	Reference Standard(s)
OTU4	2x OTL4.4	27.952493 (+/-20ppm)	NRZ Signaling, Internally Terminated, and AC Coupled	None	ITU-T G.Sup58 (10/2018) OIF-CEI-04.0 CEI-28G-VSR Very Short Reach Interface - Clause 13
	4x OTL4.2		PAM-4 Signaling, Internally Terminated, and AC Coupled	GFEC (255,239)	

Optic And Electric Specification

Table 1. Optical Specification

Parameter	Measurement Conditions	Min	Typ	Max	Unit
Transmitter					
Baud Rate	Per IQ modulator	27.95		64	Gbaud
Modulation Formats			QPSK/8QAM/ 16QAM		
Mean Modulated Output Power		-10		3	dBm
Shuttered Output Power				-35	dBm
Wavelength Range		1528.578		1567.337	nm
Frequency Range		191.275		196.125	THz
Default Channel Grid Spacing	Tunable across C-band	6.25	75	100	GHz
Channel Grid Spacing	Adjustable over C-band	0.1			GHz
Frequency Accuracy		-1.5		1.5	GHz
Frequency Fine Tune Range	Fine tuning with Tx output enabled (bright tuning)	-6		6	GHz
Lorentzian Line Width	Tx and LO			300	kHz
Tx Output Power Monitor Accuracy	Tx optical output power monitor reading relative to actual Tx output power(-15~+3dBm）	-1.5		1.5	dB
OSNR	Inband	38			dB
OSNR	Outband	34			dB
Optical Transmitter Turn On Time	Warm start			6	s

Table 1. Optical Specification

Parameter	Measurement Conditions	Min	Typ	Max	Unit
Optical Transmitter Turn On Time	Cold start			116	s
Optical Transmitter Turn Off Time	From Tx_DIS activated			10	ms
Transmitter Channel Tuning Time				86	s
Optical Return Loss	towards the module	27			dB
Receiver					
Input Power Range	100G 100ZR-OFEC-QPSK	-32		1	dBm
	100G FOIC1-OFEC-QPSK	-32			
	200G 200ZR-OFEC-QPSK	-29			
	200G 200ZR-OFEC-8QAM	-28			
	200G 200ZR-OFEC-16QAM	-24			
	200G FOIC2-OFEC-QPSK	-28			
	200G FOIC2-OFEC-8QAM	-28			
	200G FOIC2-OFEC-16QAM	-23			
	300G 300ZR-OFEC-8QAM	-23			
	300G FOIC3-OFEC-8QAM	-23			
	400G 400ZR-CFEC-16QAM	-20			
	400G 400ZR-OFEC-16QAM	-21			
	400G FOIC4-OFEC-16QAM	-20			
VOA Range	On input signal	10			dB
VOA Step Size				0.1	dB
VOA Response Time				100	ms
Signal Input Monitor Accuracy	-22dBm~+3dBm	-1.8		1.8	dB
Optical Return Loss		20			dB

Table 1. Optical Specification

Parameter	Measurement Conditions	Min	Typ	Max	Unit
OSNR Sensitivity	100G 100ZR-OFEC-QPSK			11.5	dB
	100G FOIC1-OFEC-QPSK			11.8	
	200G 200ZR-OFEC-QPSK			14.8	
	200G 200ZR-OFEC-8QAM			17.2	
	200G 200ZR-OFEC-16QAM			19.3	
	200G FOIC2-OFEC-QPSK			15.7	
	200G FOIC2-OFEC-8QAM			17.5	
	200G FOIC2-OFEC-16QAM			20	
	300G 300ZR-OFEC-8QAM			20.3	
	300G FOIC3-OFEC-8QAM			20.5	
	400G 400ZR-CFEC-16QAM			26	
	400G 400ZR-OFEC-16QAM		22	23	
	400G FOIC4-OFEC-16QAM		22	23	
CD Tolerance OSNR Penalty <0.5dB	100G 100ZR-OFEC-QPSK	80			ns/nm
	100G FOIC1-OFEC-QPSK	77			
	200G 200ZR-OFEC-QPSK	50			
	200G 200ZR-OFEC-8QAM	50			
	200G 200ZR-OFEC-16QAM	30			
	200G FOIC2-OFEC-QPSK	48			
	200G FOIC2-OFEC-8QAM	48			
	200G FOIC2-OFEC-16QAM	25			
	300G 300ZR-OFEC-8QAM	50			
	300G FOIC3-OFEC-8QAM	48			

Table 1. Optical Specification

Parameter	Measurement Conditions	Min	Typ	Max	Unit
CD Tolerance OSNR Penalty <0.5dB	400G 400ZR-CFEC-16QAM	2.4			ns/nm
	400G 400ZR-OFEC-16QAM	26			
	400G FOIC4-OFEC-16QAM	24			
SOP Tolerance OSNR Penalty < 0.5dB	100G 100ZR-OFEC-QPSK	400			krad/s
	100G FOIC1-OFEC-QPSK	400			
	200G 200ZR-OFEC-QPSK	800			
	200G 200ZR-OFEC-8QAM	70			
	200G 200ZR-OFEC-16QAM	50			
	200G FOIC2-OFEC-QPSK	800			
	200G FOIC2-OFEC-8QAM	70			
	200G FOIC2-OFEC-16QAM	50			
	300G 300ZR-OFEC-8QAM	100			
	300G FOIC3-OFEC-8QAM	120			
	400G 400ZR-CFEC-16QAM	50			
	400G 400ZR-OFEC-16QAM	80			
	400G FOIC4-OFEC-16QAM	80			
PDL Tolerance Penalty <1.3dB				3.5	dB

Interface Definition

The CFP2 module contains a PCB with a 104-contact card-edge electrical interface to external Host/Client-side logic compliant to OIF-CFP2-DCO-01.0. The network lane interface is a duplex LC connector coupled to an optical fiber carrying the DP-mQAM coherent signal in the C-band.

Table 1. Pin Descriptions

PIN	Name	I/O	Logic	Description
1	GND	GND	Ground	Module Ground. Logic and Power Return Path.
2	OHIO_RDn	O	CML	OHIO Drop inteface; Interface is Differentially AC Coupled, Internal to Module.
3	OHIO_RDp	O	CML	
4	GND	GND	Ground	Module Ground. Logic and Power Return Path
5	OHIO_TDn	I	CML	OHIO Insert Interface; Interface is Differentially AC Coupled, Terminated, and Biased Internal to Module.
6	OHIO_TDp	I	CML	
7	3.3V_GND	PWR_GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
8	3.3V_GND	PWR_GND	Ground	
9	3.3V	PWR	Power	3.3V Power Supply Input
10	3.3V	PWR	Power	
11	3.3V	PWR	Power	
12	3.3V	PWR	Power	
13	3.3V_GND	PWR_GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
14	3.3V_GND	PWR_GND	Ground	
15	NC			
16	NC			
17	PRG_CNTL1	I	3.3V LVCMOS	Internal 4.7k Pull-up; TRXIC_RSTn, TX&RX IC Reset.“0”:Reset.
18	PRG_CNTL2	I	3.3V LVCMOS	Internal 4.7k Pull-up; Hardware Interlock LSB
19	PRG_CNTL3	I	3.3V LVCMOS	Internal 4.7k Pull-up; Hardware Interlock MSB
20	PRG_ALRM1	O	3.3VLVCMOS	Programmable Alarm 1 Set over MDIO, MSA Default: HIPWR_ON, "1": Module Power Up Completed, "0": Module not High Powered Up
21	PRG_ALRM2	O	3.3V LVCMOS	Programmable Alarm 1 set over MDIO,MSA Default: MOD_READY, "1": Ready, "0": not Ready, Internally Pull-Up
22	PRG_ALRM3	O	3.3V LVCMOS	Programmable Alarm 1set over MDIO,MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND	GND	Ground	Module Ground. Logic and Power Return Path

Table 1. Pin Descriptions

PIN	Name	I/O	Logic	Description
24	TX_DIS	I	3.3V LVCMOS	Transmitter Disable, Internally Pull-Up
25	RX_LOS	O	3.3V LVCMOS	Receiver Loss of Signal
26	MOD_LOPWR	I	3.3V LVCMOS	Module Low Power Mode, Internally Pull-Up
27	MOD_ABS	O	3.3V LVCMOS	Module Absent, Internally Pull-Down
28	MOD_RSTn	I	3.3V LVCMOS	Module Reset, Active Low, Internally Pull-Down
29	GLB_ALRMn	O	3.3V LVCMOS	Global Alarm, Active Low
30	GND	GND	Ground	Module Ground Logic and Power Return Path
31	MDC	I	1.2V LVCMOS	Management Data Clock (Electrical Specsas Per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O Bi-directional Data (Electrical Specs as Per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address Bit 0
34	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address Bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address Bit 2
36	NC			
37	MSA_BER_Thresh old	O	3.3V LVCMOS	BER Threshold Signal Alarm;
38	NC			
39	3.3V_GND	PWR_GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
40	3.3V_GND	PWR_GND	Ground	
41	3.3V	PWR	Power	3.3V Power Supply Input
42	3.3V	PWR	Power	
43	3.3V	PWR	Power	
44	3.3V	PWR	Power	
45	3.3V_GND	PWR_GND	Ground	Power Ground. Internally Connected to GND. Logic and Power Return Path.
46	3.3V_GND	PWR_GND	Ground	

Table 1. Pin Descriptions

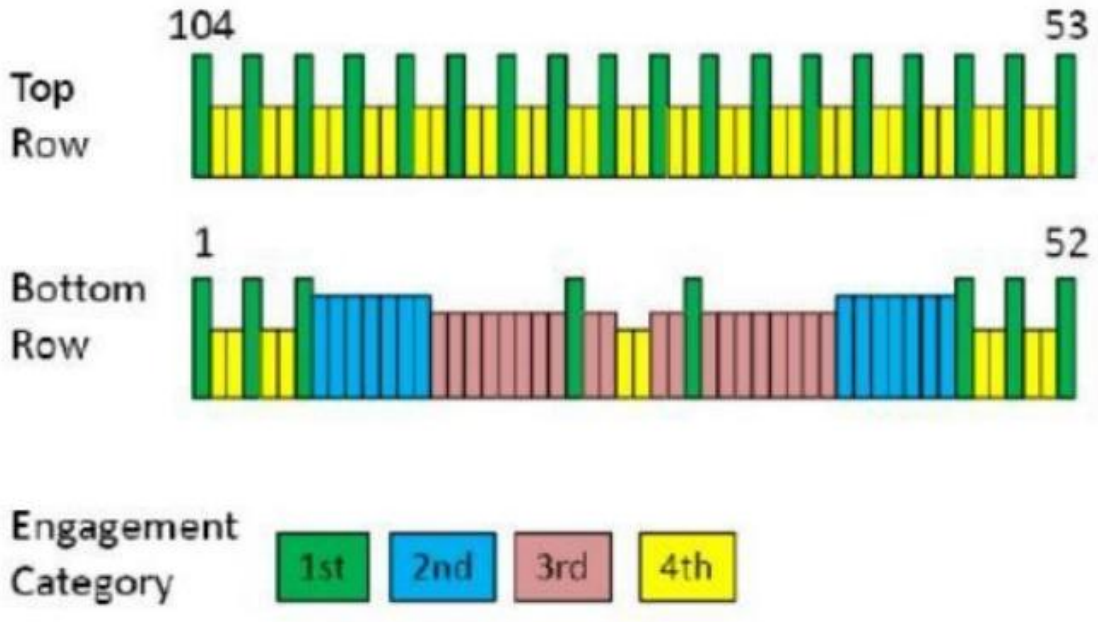
PIN	Name	I/O	Logic	Description
47	OHIO_REFCLKn	I	CML	OHIO Reference Clock: Interface is AC Coupled, Biased, and Terminated Internal to Module. If not using OHIO Interface Leave Unconnected.
48	OHIO_REFCLKp	I	CML	
49	GND	GND	Ground	Module Ground. Logic and Power Return Path
50	NC			
51	NC			
52	GND	GND	Ground	Module Ground. Logic and Power Return Path
53	GND	GND	Ground	Module Ground. Logic and Power Return Path
54	RX7p	O	CML	Host/Client RX Lane 7; Differential Signal, Internally AC Coupled.
55	RX9n	O	CML	
56	GND	GND	Ground	Module Ground. Logic and Power Return Path
57	RX0p	O	CML	Host/Client RX Lane 0; Differential Signal, Internally AC Coupled.
58	RX0n	O	CML	
59	GND	GND	Ground	Module Ground. Logic and Power Return Path
60	RX1p	O	CML	Host/Client RX Lane 1; Differential Signal, Internally AC Coupled.
61	RX1n	O	CML	
62	GND	GND	Ground	Module Ground. Logic and Power Return Path
63	RX6p	O	CML	Host/Client RX Lane 6; Differential Signal, Internally AC Coupled.
64	RX6n	O	CML	
65	GND	GND	Ground	Module Ground. Logic and Power Return Path
66	RX5p	O	CML	Host/Client RX Lane 5; Differential Signal, Internally AC Coupled.
67	RX5n	O	CML	
68	GND	GND	Ground	Module Ground. Logic and Power Return Path
69	RX2p	O	CML	Host/Client RX Lane 2; Differential Signal, Internally AC Coupled.

Table 1. Pin Descriptions

PIN	Name	I/O	Logic	Description
70	RX2n	O	CML	Host/Client RX Lane 2; Differential Signal, Internally AC Coupled.
71	GND	GND	Ground	Module Ground. Logic and Power Return Path
72	RX3p	O	CML	Host/Client RX Lane 3; Differential Signal, Internally AC Coupled.
73	RX3n	O	CML	
74	GND	GND	Ground	Module Ground. Logic and Power Return Path
75	RX4p	O	CML	Host/Client RX Lane 4; Differential Signal, Internally AC Coupled.
76	RX4n	O	CML	
77	GND	GND	Ground	Module Ground. Logic and Power Return Path
78	(REFCLKp)	N.C.	N.C.	
79	(REFCLKn)	N.C.	N.C.	
80	GND	GND	Ground	Module Ground. Logic and Power Return Path
81	TX7p	I	CML	Host/Client TX Lane 7; Differential Signal, Internally AC Coupled and Terminated.
82	TX7n	I	CML	
83	GND	GND	Ground	Module Ground. Logic and Power Return Path
84	TX0p	I	CML	Host/Client TX Lane 0; Differential Signal, Internally AC Coupled and Terminated.
85	TX0n	I	CML	
86	GND	GND	Ground	Module Ground. Logic and Power Return Path
87	TX1p	I	CML	Host/Client TX Lane 1; Differential Signal, Internally AC Coupled and Terminated.
88	TX1n	I	CML	
89	GND	GND	Ground	Module Ground. Logic and Power Return Path
90	TX6p	I	CML	Host/Client TX Lane 6; Differential Signal, Internally AC Coupled and Terminated.
91	TX6n	I	CML	
92	GND	GND	Ground	Module Ground. Logic and Power Return Path

Table 1. Pin Descriptions

PIN	Name	I/O	Logic	Description
93	TX5p	I	CML	Host/Client TX Lane 5; Differential Signal, Internally AC Coupled and Terminated.
94	TX5n	I	CML	
95	GND	GND	Ground	Module Ground. Logic and Power Return Path
96	TX2p	I	CML	Host/Client TX Lane 2; Differential Signal, Internally AC Coupled and Terminated.
97	TX2n	I	CML	
98	GND	GND	Ground	Module Ground. Logic and Power Return Path
99	TX3p	I	CML	Host/Client TX Lane 3; Differential Signal, Internally AC Coupled and Terminated.
100	TX3n	I	CML	
101	GND	GND	Ground	Module Ground. Logic and Power Return Path
102	TX4p	I	CML	Host/ClientTXLane4; Differential Signal, Internally AC Coupled and Terminated.
103	TX4n	I	CML	
104	GND	GND	Ground	Module Ground. Logic and Power Return Path



Management Interfaces

The protocol for the MSA Management Interface is IEEE 802.3 Clause 45 using the MDIO bus structure with the following additional MDIO interface specifications:

1) Support of MDC rate up to 4 MHz while maintaining downward compatibility to 100 kHz.
2) Both read and write activities occur on the rising edge of MDC clock only;
3) Supports only one MDIO device address.

Table 1. Timing parameters for Host signals

Parameter	Conditions	Min	Typ	Max	Unit
MDIO Clock Period	Time interval between two consecutive raising or falling MDC edge	250			ns
Host MDIO Set-up Time	Time interval for which Host MDIO signal must be stable prior to the sampling event of theMDC.	10			ns
Host MDIO Hold Time	Time interval for which the Host MDIO signal mustbe stable following the sampling event of the MDC	10			ns
MDC to CFP2 MDIO Delay	Time delay among MDC falling edge and CFP2 MDIO state change	0		175	ns
MOD_RSTn Assert Time	Between falling edge of MOD_RSTn and module entering Reset state			5	ms
MOD_RSTn De-assert Time	Between falling edge of MOD_RSTn and module entering Reset state			2.5	s
MOD_LOPWR Assert Time	Between rising edge of MOD_LOPWR and module entering Low-Power state			10	ms
MOD_LOPWR De-assert Time	Between falling edge of MOD_LOPWR and exit of the module from High-Power-up state			10	s
TX_DIS Assert Time	Between rising edge of TX_DIS and fall of lane output power below 10 % of nominal			100	us
TX_DIS De-assert Time	Between falling edge of TX_DIS and rise of lane output power above 90 % of nominal			20	ms
RX_LOS Assert Time	Between RX input power below LOS threshold and RX_LOS assertion			100	us
RX_LOS De-assert Time	Between RX input power above LOS threshold and RX_LOS negation			100	us
GLB_ALRM Assert Delay Time	Between occurrence of the FAWS condition and GLB_ALRMn assertion			150	ms
GLB_ALRM De-assert Delay Time	Between host clear action of FAWS latched registers and GLB_ALRMn negotiation			150	ms
PRG_ALRM Assert Time	Between occurrence of the triggering condition and alarm assertion			100	us
PRG_ALRM De-assert Time	Between end of the triggering condition and alarm negation			100	us
BERT Hardware Alarm	Between end of the triggering condition and alarm negation			100	us

High Speed Signals

The Host/Client interface high-speed signaling consists of 8 transmit and 8 receive differential pairs identified as TX[7:0][p,n] and RX[7:0][p,n]. These signals are operated in 56G PAM4 mode or 26G NRZ mode PAM4 signaling mode allows connection(s) to 1x 400G, 2x 200G, or 4x 100G Host/Client interfaces. NRZ mode allows connection(s) to 2x 100G Host/Client.

Table 1. Lane Mapping

SerDes Lanes	400G	200G	100G	
	400GAUI-8 FOIC4.8 OTUC4 (PAM4)	200GAUI-4 FOIC2.4 OTUC2 (PAM4)	CAUI-4 OTLC.4 OTL4.4 (NRZ)	100GAUI-2 OTLC.2 OTL4.2 (PAM4)
	Interface - CH[x,y]			
Tx 7[p,n];Rx 7[p,n]	CH4.1	CH2.2	CH1.2	CH1.4
Tx 6[p,n];Rx 6[p,n]				
Tx 5[p,n];Rx 5[p,n]				CH1.3
Tx 4[p,n];Rx 4[p,n]				
Tx 3[p,n];Rx 3[p,n]		CH2.1	CH1.1	CH1.2
Tx 2[p,n];Rx 2[p,n]				
Tx 1[p,n];Rx 1[p,n]				CH1.1
Tx 0[p,n];Rx 0[p,n]				

Table 2. Registers Allocation

Address	Description	Standard
8000-807F	CFP NVR1. Basic ID registers.	CFP MSA MIS V2p6r06a
8080-80FF	CFP NVR2. Extended ID registers.	CFP MSA MIS V2p6r06a
8100-817F	CFP NVR3. Network lane specific registers.	CFP MSA MIS V2p6r06a
8180-81FF	CFP NVR 4: Checksum of NVR 3 and MSA-100GLH Extended Identifiers	CFP MSA MIS V2p6r06a
8400-847F	Vendor NVR1.Vendor data registers.	CFP MSA MIS V2p6r06a
8480-84FF	Vendor NVR2. Vendor data registers.	CFP MSA MIS V2p6r06a
8500-8FFF	User private use	CFP MSA MIS V2p6r06a

Table 2. Registers Allocation

Address	Description	Standard
9000-903F	Module Control and Status Registers	
9040-91FF	Network Lane Registers	
9200-9A8F	Client Interface Registers	
9AA0-9ABF	Module Internal Status Data Block	
9AC0-9AC2	Debug Registers to Force Setting of FAWS Events	
9B00-9B37	Client Interfacex LLDP Registers	
AC00-AFFF	Common Data Block (CDB) for Command Transactions	CFP MSA MIS V2p6r06a
B000-BFFF	Coherent Module Management Interface	OIF-CFP2-ACO-01.0

Table 3. CFP2-DCO Optical Interface

Name	Type	Description
TX	LC/UPC	Optical Signal Output
RX	LC/UPC	Optical Signal Input

Operation Ratings

The table below defines the environmental specifications of the CFP2-DCO module.

Table 1. Environmental Specification

Parameter	Spec.	Unit	Note
Operating Temperature	0~+70	° C	Case Temperature
Operation Humidity	5~85	%RH	
Storage Temperature	-40~+85	° C	
Storage Humidity	5~85	%RH	

Table 2. Power Specifications

Parameter	Spec.	Unit	Note
Power Supply	3135~3465	V	
Power Supply Noise	1	%	
Operating Power Consumption	≤25	W	
Power Consumption	≤2.75	W	Low Power Mode

Ordering Information

FS P/N	Product Description
CFP2-DCO-200G-D	200G DWDM Tunable Coherent CFP2 DCO 80km DOM Duplex LC SMF Transceiver Module For Transmission, Used with D7000 Series
CFP2-DCO-400G-D	400G DWDM Tunable Coherent CFP2 DCO 80km DOM Duplex LC SMF Transceiver Module For Transmission, Used with D7000 Series

Shenzhen (China)

Address: 24F, Yingfeng Center, Haitian 2nd Rd, Nanshan District, Shenzhen
Tel: +86 (755) 8357 1351
Email: sales@feisu.com

Wuhan (China)

Address: 9-14F, Optical Valley Software Park A7, Guanshan Ave, Wuhan
Tel: +86 (027) 8808 9195
Email: sales@feisu.com

Delaware (United States)

Address: 380 Centerpoint Blvd, New Castle, DE 19720, United States
Tel: +1 (888) 468 7419
Email: us@fs.com

Birmingham (United Kingdom)

Address: Regus Edmund House, 12-22 Newhall Street, Birmingham, B3 3AS
Tel: +49 (0) 8165 4099 260
Email: uk@fs.com

Munich (Germany)

Address: NOVA Gewerbepark Building 7, Am Gfild 7,85375 Neufahrn bei Munich, Germany
Tel: +49 (0) 8165 4099 260
Email: de@fs.com

Melbourne (Australia)

Address: 57-59 Edison Rd, Dandenong South, VIC 3175, Australia
Tel: +61 3 9693 3488
Email: au@fs.com

Singapore

Address: 30A Kallang Pl, #11-10/11/12 Singapore 339213
Tel: +65 6443 7951
Email: sg@fs.com

Tokyo (Japan)

Address: JS Progress Building, 4-1-23 Heiwajima, Ota-ku, Tokyo 〒143-0006
Tel: 03-5826-8305
Email: jp@fs.com

FS has several offices around the world. Addresses, phone numbers are listed on the FS Website at https://www.fs.com/contact_us.html